MOST SIGNIFICANT BITS

CEVA TEAKLITE-4 ILLUMINATES ROADMAP

J. Scott Gardner (April 16, 2012)

Hot on the heels of introducing its XC4000 family (see *MPR 3/5/12,* "Ceva Exposes DSP Six Pack"), Ceva has lifted the curtain on another new family of DSP cores. Speaking at the Linley Tech Mobile Conference, the company announced its new TeakLite-4 architecture and provided details about four new cores it plans to launch this year. As the successor to its popular TeakLite-III family, the software-compatible architecture is designed to scale across a broad range of product categories. TeakLite-4 DSPs will primarily target audio and voice processing in everything from low-power mobile devices to high-end home entertainment systems.

TeakLite-4 is similar to TeakLite-III, but its microarchitecture is much more flexible. It allows developers to customize the instruction-set architecture (ISA), memory hierarchy, and I/O interfaces. It retains TeakLite-III's 10-stage pipeline and still issues three instructions per clock cycle, but extra computational units allow up to six operations per cycle. Ceva tuned the pipeline to balance performance and enable logical isolation for different blocks and register files. Design scalability eases offloading of computation to accelerators for better power efficiency or higher performance. Using optional master/slave ports and dedicated extension ports, data can flow to and from other DSPs or tightly coupled coprocessors.

TeakLite-4 includes several enhancements to increase power efficiency, including version 2.0 of Ceva's power-qa_jgle unit that reduces both dynamic and leakage power. The design enables better power management with more granularity to control the power and performance of DSP subsystems. Ceva expects TeakLite-4 to operate at clock speeds of up to 1.5GHz (worst case) in TSMC's 28nm high-performance mm`gjc (HPM) process.

Scheduled for release in May, the Ceva-TL410 is the first TeakLite-4 core. It is designed for the low end of the audio market (e.g., audio codecs and noise-reduction chips), consuming less power than TeakLite-III and requiring less logic (only 100,000 gates when optimized for area). The DSP has a single 32x32-bit multiply-accumulate (MAC) unit and dual 16x16-bit MAC units. To reduce size and power, optional Teaklite-4 instructions can be eliminated. The interface to data memory is 64 bits wide, and the design does not require an external system bus; all data can be transferred using the native DSP memory ports.

The TL410 matches the audio-processing performance of TeakLite-III while requiring 80% of the die area (when area optimized) and 70% of the application power for MP3 decoding (when manufactured in 28nm HPM). Available simultaneously, the Ceva-TL420 adds on top of the TL410 a cached-memory subsystem with master/slave AXI ports, targeting application processors as well as DTV and STB main SoCs.

In September, the company plans to release the Ceva-TL411 and Ceva-TL421 cores, which target the midrange to high-end audio-DSP market. These DSP cores support mobile designs while doubling the number of MAC units over the TL4x0 and introducing new instructions and mechanisms for efficient audio decode. The dual 32x32-bit MACs and quad 16x16-bit MACs are fed by a 64-bit data bus. Designers may also integrate an optional floating-point unit to improve dynamic range in audio-processing algorithms. Compared with TeakLite-III, the TL411 uses about 10% more die area, but it requires only 45% of the application power when executing an advanced audio-postprocessing algorithm such as Dirac HD Sound.

The TeakLite-4 architecture can be extended even further to allow Ceva to address high-end audio processing in products that are less power sensitive, such as digital TVs and game consoles. The designers can add two additional 32x32-bit MAC units for a total of four, matching the number of 16x16-bit MAC units. To balance system bandwidth in order to support the extra computational horsepower, the architecture can widen the data-memory interface to 128 bits. TeakLite-4 supports optional features that include cache controllers, ISA extensions (such as entropy encoding), and accelerators in the form of tightly coupled coprocessors (including customer-specific designs). The base core for a quad-MAC implementation would be approximately 50% larger than TeakLite-III, but Ceva expects performance to improve by up to 4–6x.

Ceva's TeakLite-4 family will compete with Tensilica's HiFi family (see *MPR 2/6/12,* "Tensilica's HiFi 3 Sounds Good"), but Tensilica lacks preconfigured cores to serve such a wide range of applications. Future products using the TeakLite-4 architecture could support twice as many 32x32-bit MACs and deliver twice the data bandwidth of Tensilica's HiFi 3. Even Ceva's low-end TL410 (and TeakLite-III) supports native 32-bit precision, a feature Tensilica didn't offer until HiFi 3 (released in March).

Ceva's audio roadmap is now firm for the next few quarters, at least for standard IP products. The company can also use the TeakLite-4 architecture to create custom designs for key customers. Surprisingly, the performance needs for audio processing continue to increase. Ceva has created a scalable architecture that should address every conceivable DSP audio application, but the developers of audio algorithms will no doubt find new compute-intensive ways to manipulate sound waves—regardless of whether most people can hear the difference. ♦