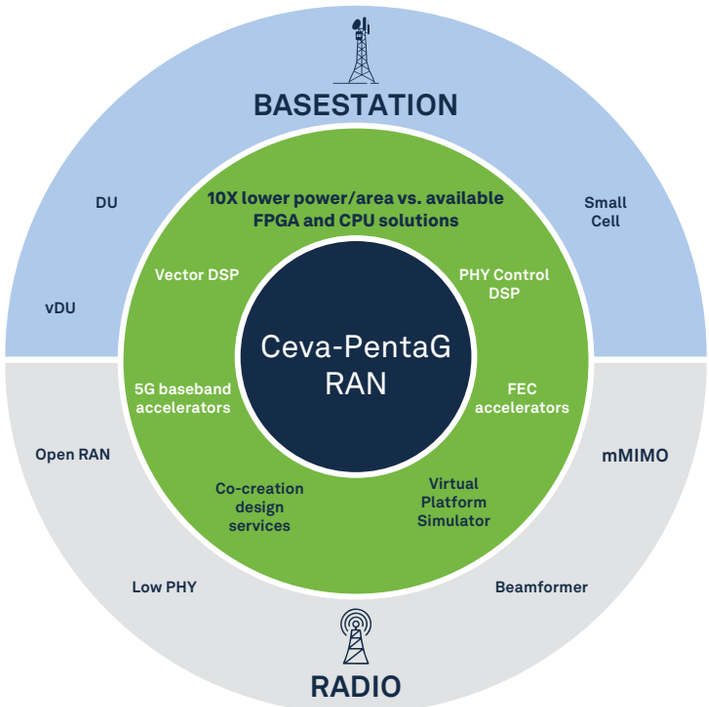
5G MOBILE & INFRASTRUCTURE

CONTENT LIST

Baseband Platform IP for 5G RAN ASICs

Ceva-PentaG RAN is industry's most comprehensive and integrated baseband Platform IP targeting base stations, radio devices, Open-RAN and Massive MIMO devices



Key Benefits

- Heterogeneous compute platform comprising best in class Ceva-XC Vector
- DSPs and 5Goptimized HW accelerator blocks
- Platform configurations supporting both DU/Baseband and Radio Unit SoCs
- Optimal HW/SW partitioning with completeprocessing chain acceleration (PUSCH, PUCCH, PDSCH)
- Delivers 10x power savings compared to FPGA and other COTS alternatives
- Comprehensive and flexible solution addressing wide range of infrastructure use cases and form factors
- Scalable and efficient Massive MIMObeamforming computing
- VPS - unique System-C Virtual PlatformSimulator, modeling all platform components, allowing fast prototyping, proof of concept,pre-silicon SW development, and solution dimensioning

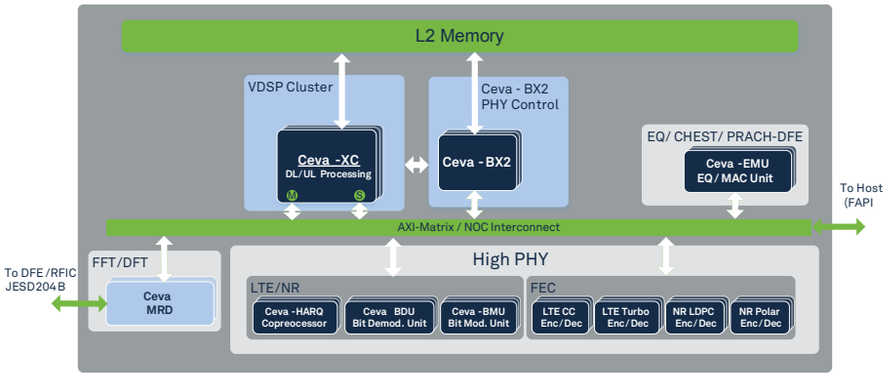
Reducing TTM, risk, effort and cost for 5G RAN SoC development

SoC co-creation design service offering, fromarchitecture to GDS and test chips

Applications and use-cases

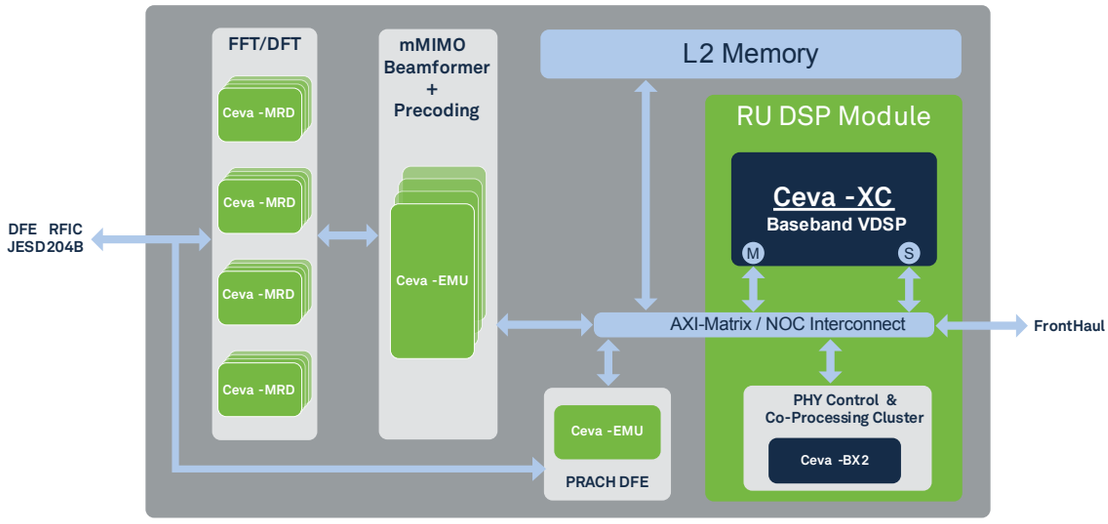
- 5G-NR & LTE base station
  - DU and O-DU
  - Inline DU acceleration
  - Baseband compute chiplets
  - Virtual RAN
  - Open RAN supporting 7.2x splits
  - Small-Cell split 6 & 2
  - NTN
- Radio Units
  - O-RU
  - Low-PHY Sub-systems
  - Digital integration into transceivers
  - Massive MIMO Beamforming
  - Millimeter Waves

Ceva-PentaG RAN DU/Small Cell Platform



Ceva-PentaG RAN Block diagram

Ceva-PentaG RAN Radio Platform



The Key Aspects of Ceva-PentaG RAN

Using best in class and market proven vector DSPs	Leveraging a long legacy in cellular infrastructure, and widely used in mass production in
Complete Acceleration of Major Processing Chains	End-to-end acceleration of downlink and uplink processing chains, achieving unparalleled power efficiency
Scalable and Flexible	Highly flexible architecture, allowing customers to dimension their solution using Ceva-PentaG RAN building blocks, with standard AXI/APB interfaces, and add their own IP and secret sauce
Rich Set of HW Accelerators	Heterogeneous platform covering all processing chain components, including FFT, Equalization,Symbol/Bit Modulation and Demodulation, HARQ, and 4G/5G FEC Encoding and Decoding
Solving Massive MIMO Compute challenge	For both DU and RU side processing. Scalable acceleration of Beamforming data-path. Efficient compute of large dimension beam forming weights
Virtual Platform Simulator	Modeling all Ceva-PentaG RAN accelerators and DSP cores, allowing pre-silicon SW development fast prototyping, PoC and solution dimensioning
SoC Co-Creation Design Service Offering	Customizing service offering for customer's use case, from architecture to GDS

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For more information:

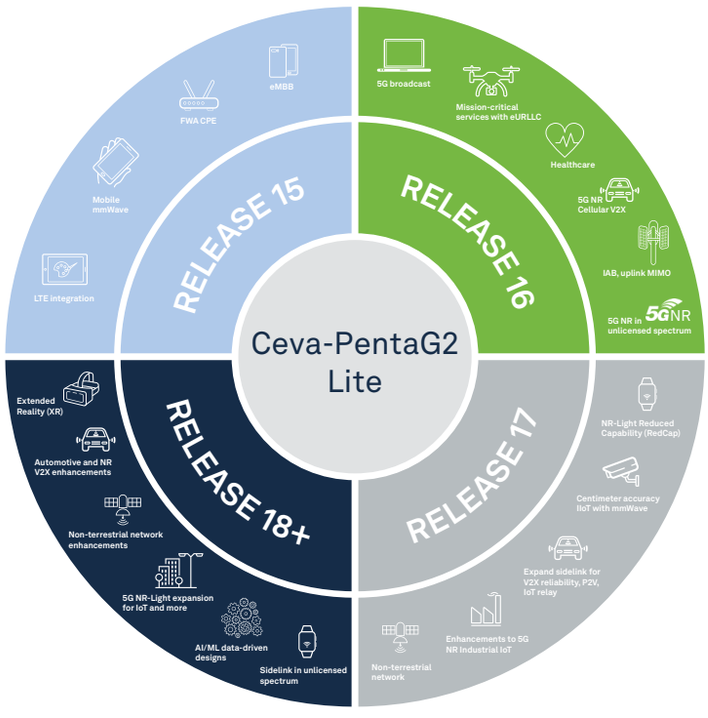
Integrative baseband IP platform for Cellular IoT

Ceva-PentaG2 Lite is industry's first comprehensive and integrative baseband IP Platform meeting challenging tight power envelope targets for next generation cellular IoT devices, supporting LTE Cat.1 and future 5G RedCap devices

Key Benefits

- Lean and compact architecture, supporting reduced capacity use cases
- Supporting a range of BW configurations, from Rel 17 20MHz, to future Rel 18 5/10MHz, and 1 or 2 antennas option
- Complete acceleration of all major processing chains for both downlink and uplink, achieving extreme power consumption constraint targets
- Flexible and customizable baseband platform, with optimal HW/SW partitioning using a single scalar DSP controller and HW accelerators
- Optimized and efficient HW accelerators for FFT, Equalization, Bit/Symbol modulation and demodulation, and FEC
- Leveraging industry proven small footprint Ceva-BX2 as PHY controller DSP, able to run the protocol stack as well for tight Integration
- Reference end-to-end SW Implementation of major processing chains, Including PDSHC, PDCCH, PUSCH
- Comprehensive System-C SoC simulator, modeling all platform components, demonstrating major processing chains (HW+SW), allowing fast prototyping, proof of concept and solution dimensioning
- Second generation and scaled down version of Ceva-PentaG2 architecture, reducing TTM, risk, effort and cost for new SoC development

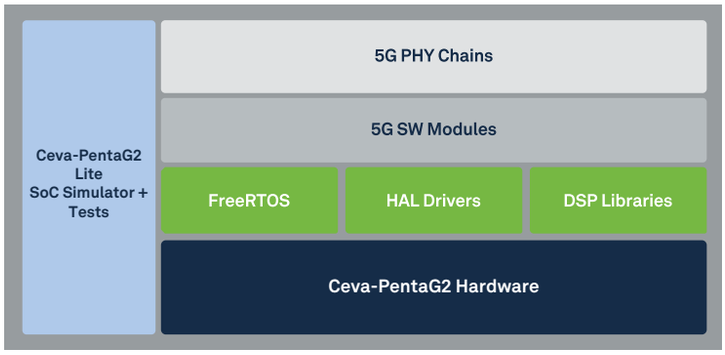
Ceva-PentaG2 - Target Applications Diag



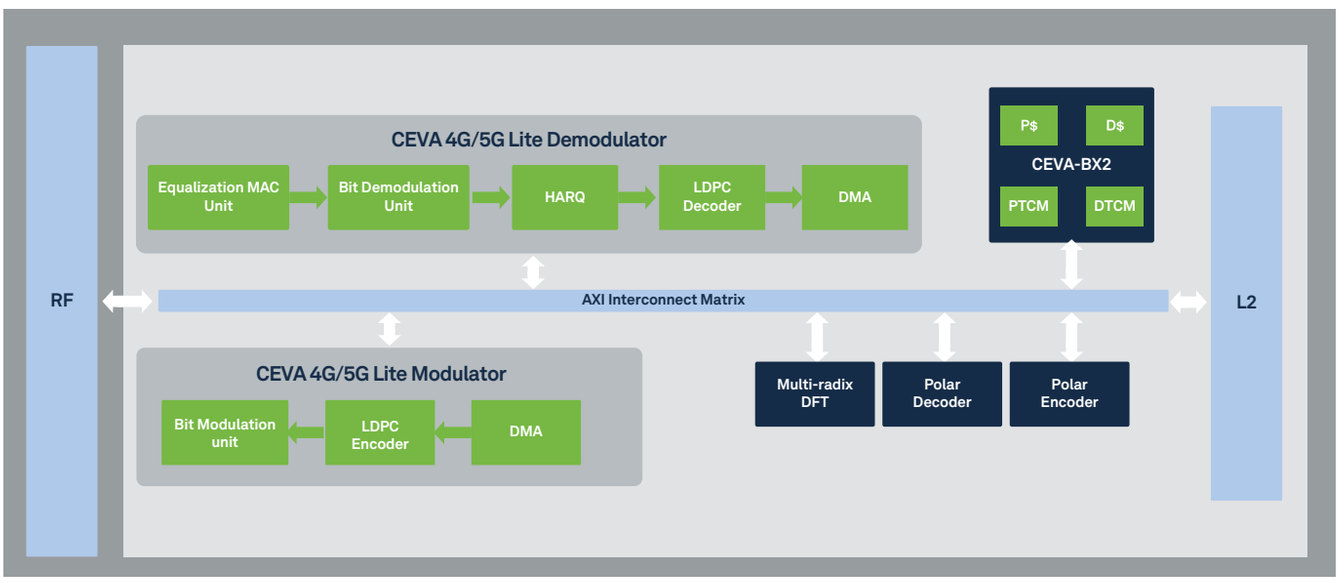
Applications and use-cases

- 5G-NR & LTE UE low power devices
  - 5G RedCap (a.k.a. NR-Lite)
  - LTE Cat1 to Cat4
  - Wearables
  - Surveillance cameras
  - Industrial sensing
  - Car telemetry
  - M2M Modules
  - Asset tracking
  - Share bike

Ceva-PentaG2 Lite deliverables



Ceva-PentaG2 Lite Block Diagram



The Key Aspects of Ceva-PentaG2 Lite

Optimized lean and compact Baseband Solution	Achieving aggressive power consumption and area targets for low cost battery powered IoT devices
Complete Acceleration of Major Processing Chains	End-to-end acceleration of downlink and uplink processing chains, for both LTE Cat.1 and future 5G RedCap, re-using the same platform
Scalable and Flexible	Highly Fexible architecture, allowing customers to dimension their solution using PentaG2 Building blocks, with standard AXI/APB interfaces, and add their own IP and secret sauce
Rich Set of HW Accelerators	Covering all processing chain components, including FFT/IFFT, Equalization, Symbol/Bit Modulation and Demodulation, HARQ, and 4G/5G FEC Encoding and Decoding
Low footprint DSP controller	Using field proven Ceva-BX2 scalar DSP for tightl;y coupled PHY control and HW accelerator sequencing. Can be used for running Protocol Stack as well
End-to-end 5G Processing Chains SW and libraries	Standard compliant reference implementation of major processing chains, including PDSCH, PDCCH, PUSCH, augmented with rich set of optimized 5G libraries
Comprehensive SoC Simulator	Modeling all Ceva-PentaG2 Lite accelerators and DSP core, allowing pre-silicon SW development fast prototyping, PoC and solution dimensioning

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For more information:

Ceva-PentaG™ PRODUCT NOTE

World's most advanced Baseband IP platform for Mobile Broadband 5G

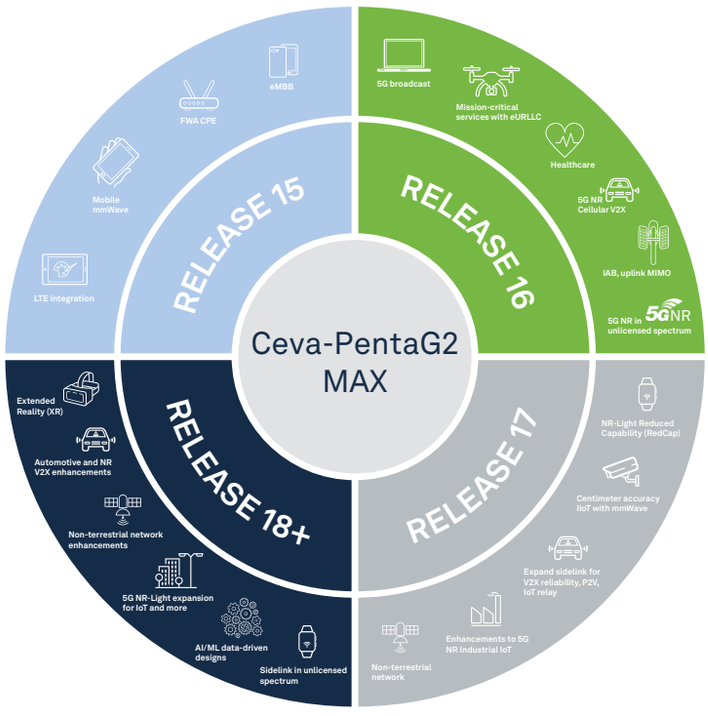
Ceva-PentaG2 Max is industry's most comprehensive IP Platform capable of meeting the extreme low latency, and strict power budget for 3GPP 5G UE broadband eMBB and URLLC devices

Key Benefits

- Fully configurable IP platform for 5G NR and legacy 4G multi-mode RAT, targeting both
- Scalable and customizable heterogeneous compute platform, with optimal HW/SW partitioning using a set of vector and scalar DSPs, co-processors and HW accelerators for achieving customer power and performance target

  Complete inline acceleration of all major processing chains for both downlink and uplink
- Optimized HW accelerators for FFT, Equalization, Bit/Symbol modulation and demodulation, MLD, and FEC
- Leveraging industry proven Ceva-XC4500 vector baseband DSP with 5G ISA extensions
- Reference end-to-end SW Implementation of major processing chains, Including PDSHC, PDCCH, PUSCH
- Comprehensive System-C SoC simulator, modeling all platform components, demonstrating major processing chains, allowing fast prototyping, proof of concept and solution dimensioning
- Second generation of PentaG architecture, reducing TTM, risk, effort and cost for new SoC development

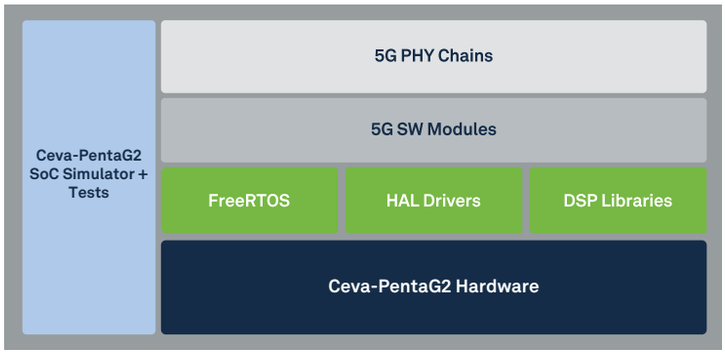
Ceva-PentaG2 - Target Applications Diagram



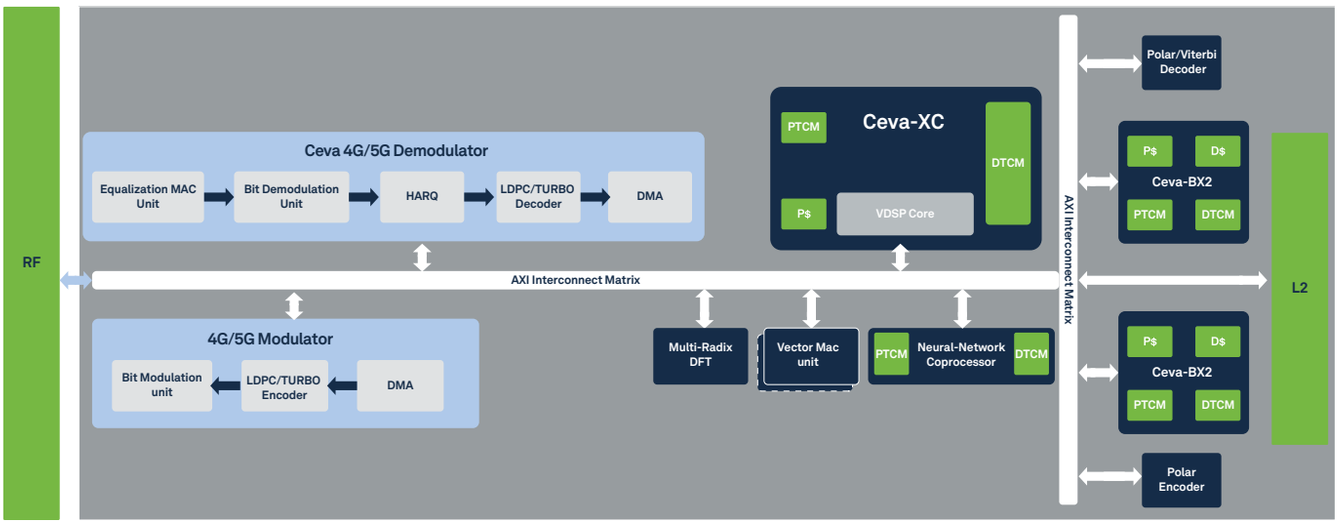
Applications and use-cases

- 5G-NR & LTE UE devices
  - Handsets and Cellular baseband
  - Notebook datacard
  - FWA (Fixed Wireless Access) and CPE
  - XR & Headsets
  - Mission Critical
  - C-V2X (Cellular V2X)
  - Repeaters and IAB

Ceva-PentaG2 MAX deliverables



Ceva-PentaG2 Max Block Diagram



The Key Aspects of PentaG2-Max

Enhanced Ceva-XC4500 DSP with 5G ISA Extensions	Field-proven DSP with new 5G ISA extensions specifically designed to accelerate key functions in the modem. Customer extendable using Ceva-Xtend
Ceva-BX2 scalar DSPs	Multiple Ceva-BX2 cores designed to address high performance and ultra-low latency demands of 5G PHY control.
Vector MAC Unit (VMU) Co-Processor	64 MAC co-processor designed to handle advanced channel estimation measurements and schemes in multiple channels.
TCEs and Accelerators	A set of HW accelerators, including FEC encoders/decoders, FFTs, MLD (LTE), etc.
NNCP AI Processor	Designed to handle advanced beamforming techniques and link adaptation scenarios using neural networks.
System-level Simulation	An integrated C-level simulation environment that allows system engineers, architects and SW developers to model, pro le and debug at cycle-accurate system level.
SW libraries and chains	A rich set of DSP, Comm and 5G libraries, as well as complete reference chains (e.g. PDCCH receiver)

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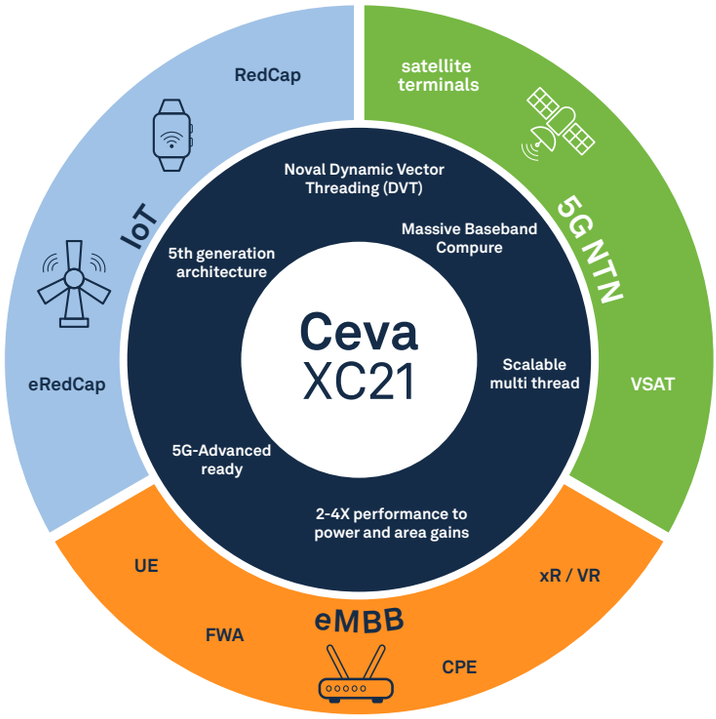
For more information:

Ceva-XC21 is enabling next generation 5G-Advanced and 6G modems with highly efficient communication DSP

Ceva-XC21 is a DSP core based on the fifth generation Ceva-XC20 vector processor architecture. Ceva-XC21 5G IoT DSP designed for low-power, cost- and size-optimized cellular IoT modems, RedCap, eRedCap, NTN VSAT terminals, eMBB and uRLLC applications. It is highly scalable multi-threaded vector processor that enables system designers to optimize silicon size, power and performance to their applications needs.



Key Benefits

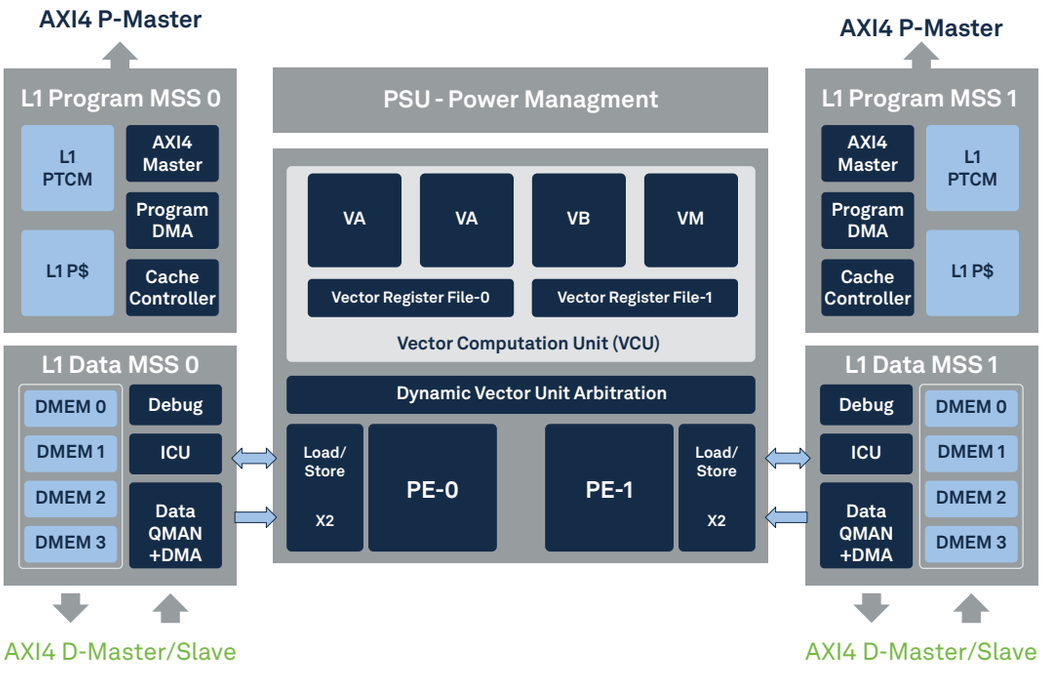
- Unparalleled compute efficiency employing Dynamic Vector Threading (DVT) true vector multi-thread technology
- Two execution threads dynamically sharing advanced Vector Compute Unit (VCU) resources
- Integrated into Ceva's PentaG Cellular Platforms
- High parallelism vector processing based on VLIW model
- New high performance scalar processor with 5.14 CoreMark/ MHz
- Scalability: MAC configurations of 32 or 64 with a single thread and dual thread option
- AI workloads support with INT8/INT16 data type
- Support 5G ISA for NR physical layer acceleration & efficiency
- Integrated DMA and QMAN (Que Manager) for low latency, minimal SW overheads data transfer
- Mature and advanced LLVM SW tools for code size and cycle count efficiency
- Code compatibility with legacy XC4500 DSP

Applications and use-cases

- UE and Terminals
  - IoT UE: RedCap / eRedCap
  - CAT M / CAT1 / CAT4
  - 5G NTN Terminals

	Parameter	XC4500 (Reference)	XC210	XC211	XC212
Product Specifications	Scalar Architecture	2nd generation	3rd generation scalar processor with 40% performance boost		
	Threads (# of PE)	Single			Dual
	SIMD Vector Size	512	256		
	MACs (16x16)	64	32	64	
	Features	4G/5G	5G-Advanced ISA, AI support (INT8 data type), Dynamic Vector Threading, 3D DMA		
	Design target		Cost optimized	Balanced	Highest performance efficiency

Ceva-XC21 block diagram



Architecture Highlights

- Dual execution threads, each with its independent Program and Memory sub-systems
- Dynamic Vector Threading – per cycle arbitration on VCU resources
- Unmatched vector efficiency
- Best in class 2048-bit memory bandwidth, 1024-bit per thread, with two load/store units per thread
- 8-way VLIW provides optimal hardware utilization
- Enhanced VCU, with two Vector Arithmetic units, Vector Non-Linear and Vector Move/Scale, all in parallel
- Advanced program L1 Cache plus TCM support, per execution core
- Local Dara Memory – 4 blocks allowing uncontended access for the two execution cores and external DMAs
- Third generation dual multi thread Scalar PE (Processing Element) with optimized LLVM compiler for code size and performance
- PE supports very low overhead RTOS multi-tasking with dynamic branch prediction
- Core streaming interfaces support ultra-low latency
- AMBA 4 compliant matrix interconnect
- Multidimensional DMA with advanced Queue manager for uninterrupted data movement into and out of the core, using optional auxiliary wide AXI interfaces
- Custom ISA extension for the scalar and vector processing unit leveraging Ceva-Extend interface
- Designed for low power with automatic clock stops, light sleep mode and standby mode
- Simulation and emulation: instruction accurate and cycle accurate simulators

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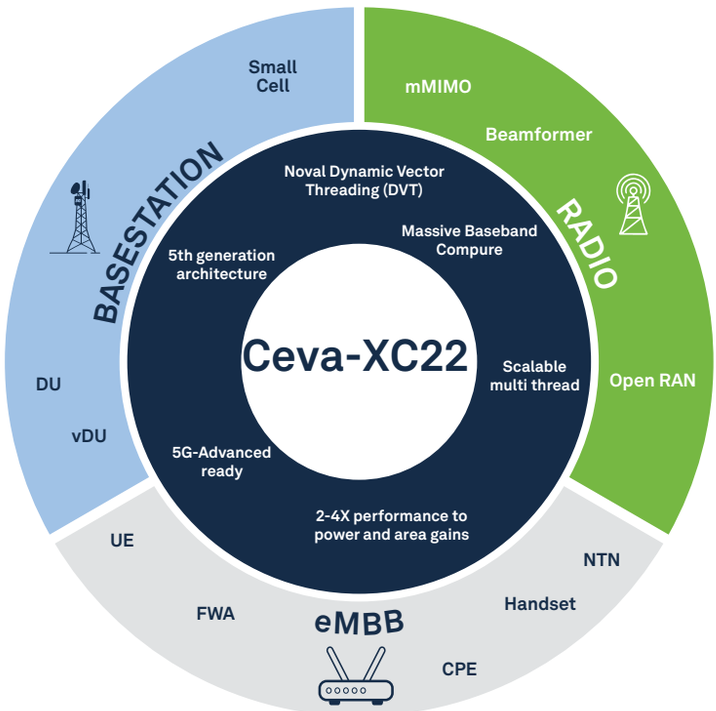
For more information:

Enabling next generation 5G-Advanced - world's most powerful vector DSP for cellular baseband applications

Ceva-XC22 is the first DSP core based on the fifth generation Ceva-XC20 vector processor architecture from Ceva, designed to address 5G-Advanced compute challenges. It is a scalable vector multi-thread processor, targeted for advanced 5G RAN and high-end UE terminals, from Basestations and Massive MIMO Radios to next generation CPE and FWA terminals.

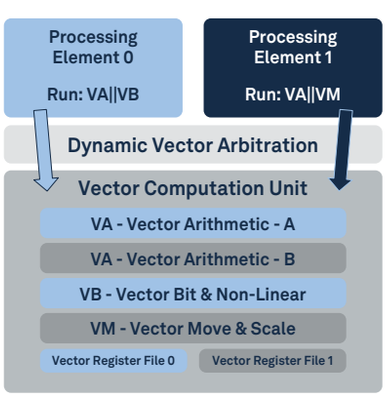


Key Benefits

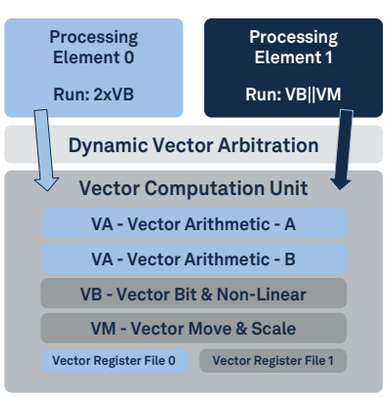
- Unparalleled compute efficiency employing Dynamic Vector Threading (DVT) true vector multi-thread technology
- Two execution threads dynamically sharing advanced Vector Compute Unit (VCU) resources
- Dual advanced Data and Program Memory Subsystems
- Dual load/store units per thread, supporting total of 2048-bit width access to memory
- Employing 128 MAC units and achieving dramatic 2.5X efficiency improvement relative to previous generation
- Integrated into Ceva's PentaG Cellular Platforms

Applications and use-cases

- Cellular Infrastructure:
  - Basestations
  - vDU acceleration
  - Small Cells
  - Massive MIMO and Beamforming RRU
  - Open RAN compute
- Advanced UE devices and Terminals:
  - Fixed Wireless Access and CPE
  - eMBB and carrier aggregation
  - Next generation 5G-Advanced terminals

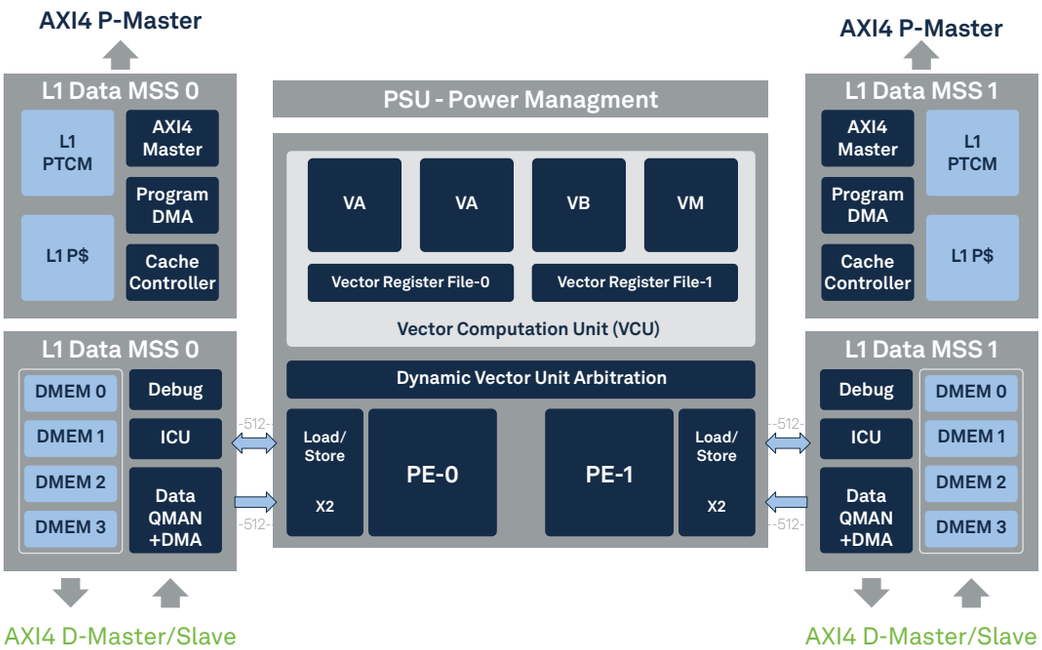


DVT Arbitration Example 1
(symetric VA allocation)



DVT Arbitration Example 2
(wide VA allocation)

Ceva-XC-22 block diagram



Architecture Highlights

- Dual execution threads, each with its independent Program and Memory sub-systems
- Dynamic Vector Threading – per cycle arbitration on VCU resources unmatched vector efficiency
- Best in class 2048-bit memory bandwidth, 1024-bit per thread, with two load/store units per thread
- 8-way VLIW provides optimal hardware utilization
- Enhanced VCU, with two Vector Arithmetic units, Vector Non-Linear and Vector Move/Scale, all in parallel Advanced program L1 Cache plus TCM support, per execution core
- Local Dara Memory – 4 blocks allowing uncontended access for the two execution cores and external DMAs
- Third generation dual multi thread CPU/DSP Scalar PE (Processing Element) with optimizing C compiler for protocol, control, and DSP native C code
- PE supports very low overhead RTOS multi-tasking with dynamic branch prediction
- Massive number of IoT/MTC users served by control plane
- Core streaming interfaces support ultra-low latency
- AMBA 4 compliant matrix interconnect
- Comprehensive multicore support with ACE-compliant cache coherency
- Multidimensional DMA with advanced Queue manager for uninterrupted data movement into and out of the core, using optional auxiliary wide AXI interfaces

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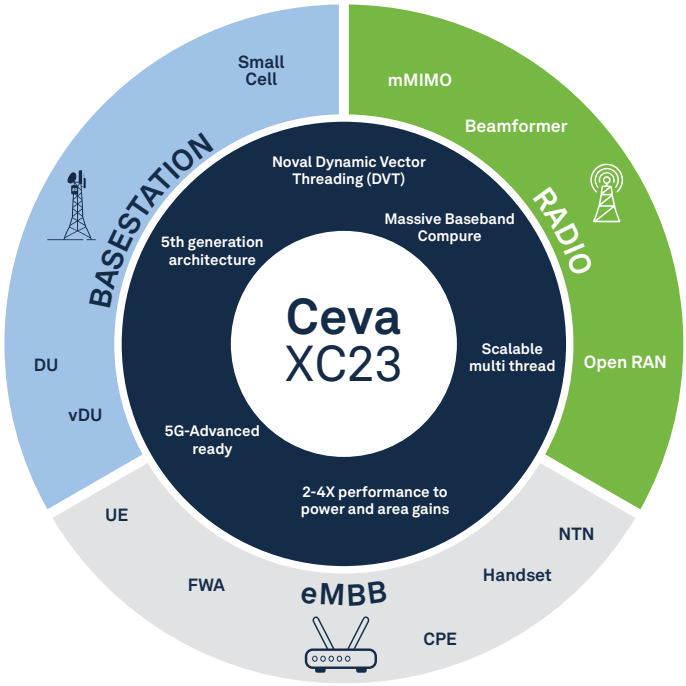
For more information:

Enabling next generation 5G-Advanced & 6G world's most powerful vector DSP for cellular baseband applications

Ceva-XC23 is the first DSP core based on the fifth generation Ceva-XC20 vector processor architecture from Ceva, designed to address 5G & 6G compute challenges. It is a scalable vector multi-thread processor, targeted for advanced 5G RAN and high-end UE terminals, from Basestations and Massive MIMO Radios to next generation CPE and FWA terminals.

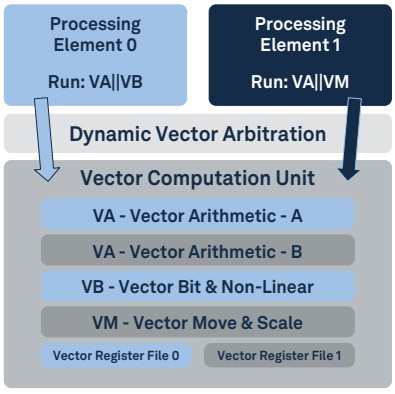


Key Benefits

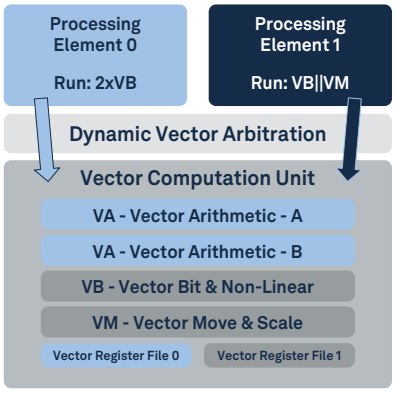
- Unparalleled compute efficiency employing Dynamic Vector Threading (DVT) true vector multi-thread technology
- Two execution threads dynamically sharing advanced Vector Compute Unit (VCU) resources
- Dual advanced Data and Program Memory Subsystems
- Dual load/store units per thread, supporting total of 2048-bit width access to memory
- Employing 128 MAC units and achieving dramatic 2.5X efficiency improvement relative to previous generation
- Integrated into Ceva's PentaG Cellular Platforms
- New high performance scalar processor with 5.14 CoreMark/ MHz
- AI workloads support with INT8/INT16 data type
- Support 5G ISA for NR physical layer acceleration & efficiency
- Integrated DMA and QMAN (Que Manager) for low latency, minimal SW overheads data transfer
- Mature and advanced LLVM SW tools for code size and cycle count efficiency
- Code compatibility with legacy XC4500 DSP

Applications and use-cases

- Cellular Infrastructure:
  - Basestations
  - vDU acceleration
  - Small Cells
  - Massive MIMO and Beamforming RRU
  - Open RAN compute
- Advanced UE devices and Terminals:
  - Fixed Wireless Access and CPE
  - eMBB and carrier aggregation
  - Next generation 5G-Advanced terminals

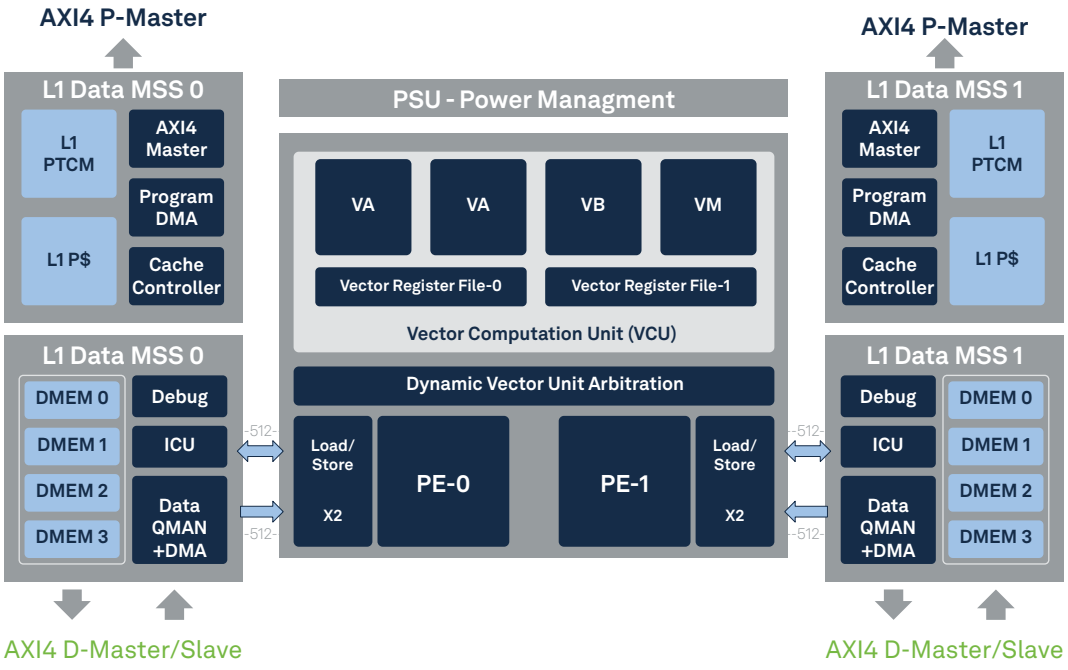


DVT Arbitration Example 1
(symetric VA allocation)



DVT Arbitration Example 2
(wide VA allocation)

Ceva-XC23 block diagram



Architecture Highlights

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- Enhanced VCU, with two Vector Arithmetic units, Vector Non-Linear and Vector Move/Scale, all in parallel
- Advanced program L1 Cache plus TCM support, per execution core
- Local Dara Memory – 4 blocks allowing uncontended access for the two execution cores and external DMAs
- Third generation dual multi thread CPU/DSP Scalar PE (Processing Element) with optimizing C compiler for protocol, control, and DSP native C code
- PE supports very low overhead RTOS multi-tasking with dynamic branch prediction
- Core streaming interfaces support ultra-low latency
- AMBA 4 compliant matrix interconnect
- Multidimensional DMA with advanced Queue manager for uninterrupted data movement into and out of the core, using optional auxiliary wide AXI interfaces
- Custom ISA extension for the scalar and vector processing unit leveraging Ceva-Extend interface
- Designed for low power with automatic clock stops, light sleep mode and standby mode
- Simulation and emulation: instruction accurate and cycle accurate simulators

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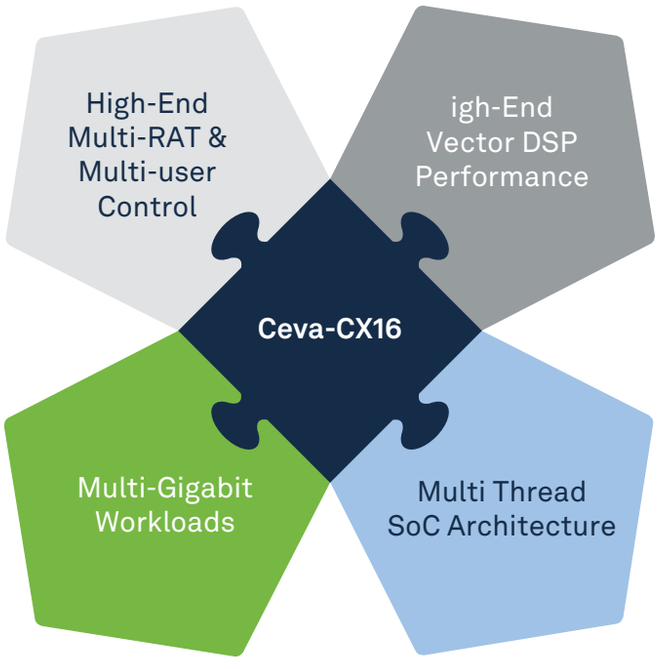
For more information:

Enabling next generation 5G RAN - world's strongest vector DSP for cellular baseband applications

Ceva-XC16 is sixth generation vector processor IP from Ceva, designed to bring multi-gigabit high-end communication and cellular capabilities to base-stations, small-cells, gateways, access points and CPEs.

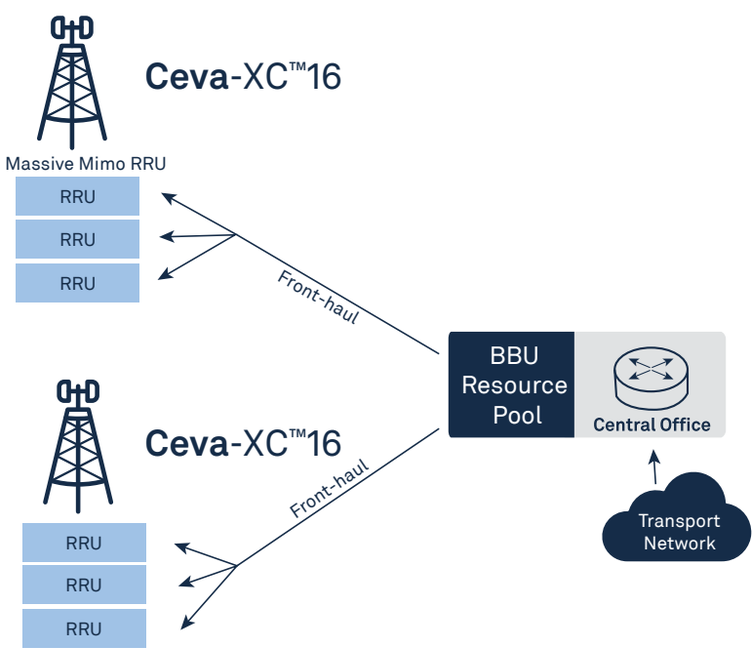


Key Benefits

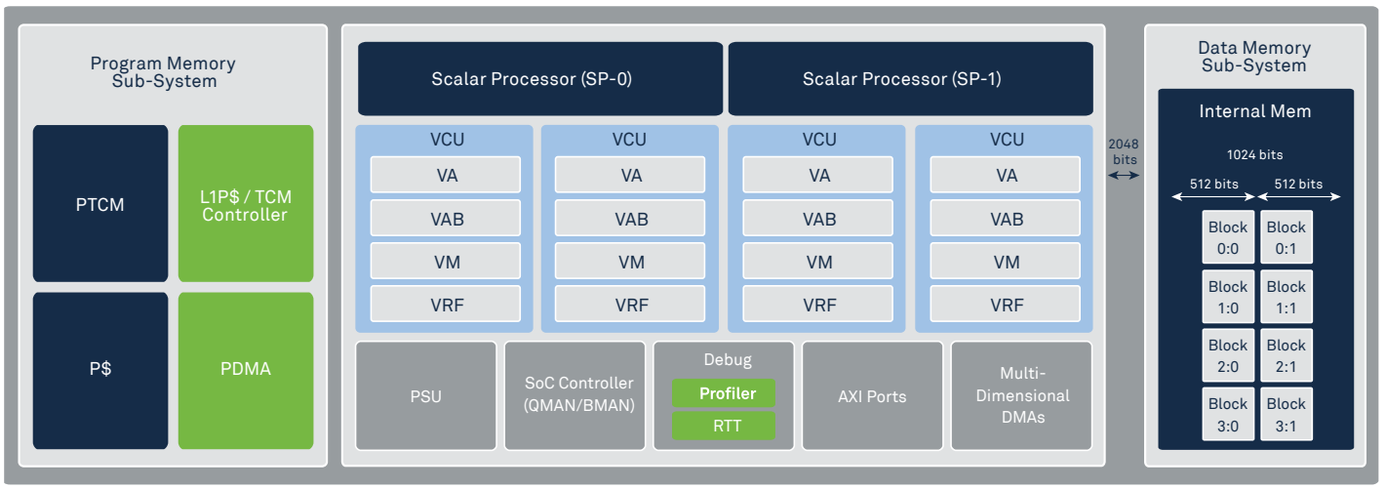
- **Meets the demanding requirements** of extreme multi-gigabit communications use cases and large-scale baseband aggregation
- **Scalable architecture** addresses the full range of eNodeB and gNB from femtocell, small cell, macrocell, BBU & RRH to Cloud-RAN
- **Quad-vector processor addresses** the needs of next-generation wireless applications such as 5G-NR, FWA, C-V2X, Wi-Fi 6 (802.11ax)
- **Dual-scalar processor** running simultaneous multi thread, third generation Ceva scalar architecture with superior code size
- **Enhanced Multi-User** capabilities, supporting dynamic massive single user and fine multi user allocations

Applications and use-cases

- **5G-NR & LTE-A Pro infrastructure**
  - Cloud-RAN, V-RAN, DU acceleration, BBU aggregation, Massive MIMO RRH, Massive Carrier Aggregation RRH, Macrocell, Small Cell, and IAB (Integrated Access and Back-haul), eCPRI compression and management
  - FWA (Fixed Wireless Access) and CPE
  - Supporting 3GPP Release 16 and 17 use cases, in both eMBB and uRLLC



Ceva-XC16 architecture diagram



Architecture Highlights

- **Core Features**
  - Fully programmable DSP architecture incorporating unique mix of VLIW and SIMD vector capabilities Increased length pipeline enables unprecedented vector unit speeds, architected for advanced process nodes – up to 1.8GHz
  - Best in class 2048-bit memory BW
  - 8-way VLIW provides optimal hardware utilization
  - Extremely powerful quad vector processor supports fixed- and floating-point operations with 256 MACs per cycle
  - Dynamic allocation of vector units to scalar processors
  - Unique high-precision arithmetic optimized for matrix processing up to 256x256 and for non-linear operators
  - Fully redesigned third generation dual multi thread CPU/DSP SPU (Scalar Processing Unit) with optimizing Ccompiler for protocol, control, and DSP native C code
  - SPU supports very low overhead RTOS multi-tasking with dynamic branch prediction
  - Massive number of IoT/MTC users served by control plane
- **System features**
  - Core streaming interfaces support ultra-low latency
  - AMBA 4 compliant matrix interconnect
  - Comprehensive multicore support with ACE-compliant cache coherency
  - Advanced high-bandwidth memory subsystem for efficient utilization of vector unit
  - Hardware/software partitioning delivers exceptional power efficiency while maintaining software flexibility with Queue and Buffer Managers and AXI interfaces

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For more information:

Enabling SDR based, very low power multi-gigabit mobile communications

Ceva-XC4500 is the fourth generation vector processor IP from Ceva, designed to bring very low power, multigigabit, wireless modems capabilities to 5G-NR, LTE-A Pro and WiFi UE, CPE and Access Points.

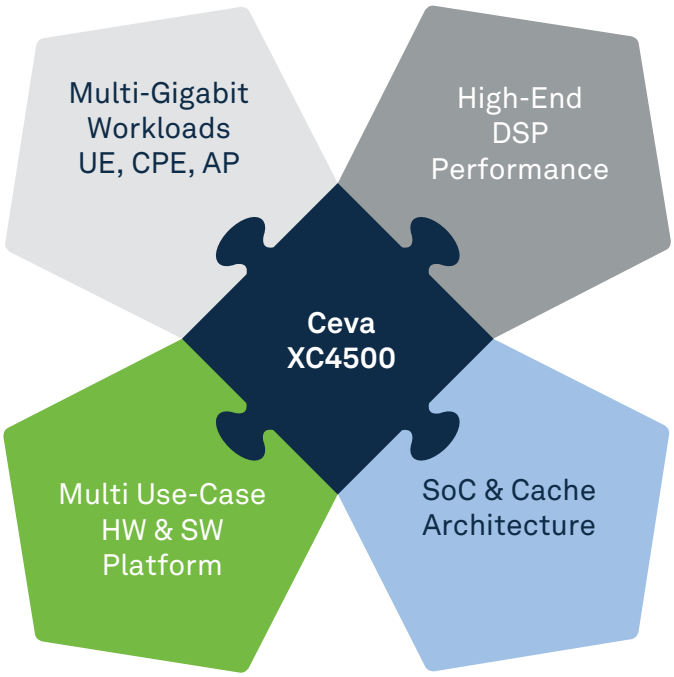
Key Benefits

- **Meets the demanding requirements** of very low power multi-gigabit mobile modem use cases
- **Reduces Time To Market with Ceva-XC4500** based platform that includes a rich set of HW accelerators combined with extensive optimized SW communication libraries for all celluar standards
- **Extendible and versatile architecture** addresses gigabit modems for 5G-NR eMBB, Fixed wireless access CPE, Cellular-V2X and 802.11p DSRC, Wi-Fi 11ax/ac 4x4 & 8x8 MS and AP, and Automotive Radar & Lidar

Applications and use-cases

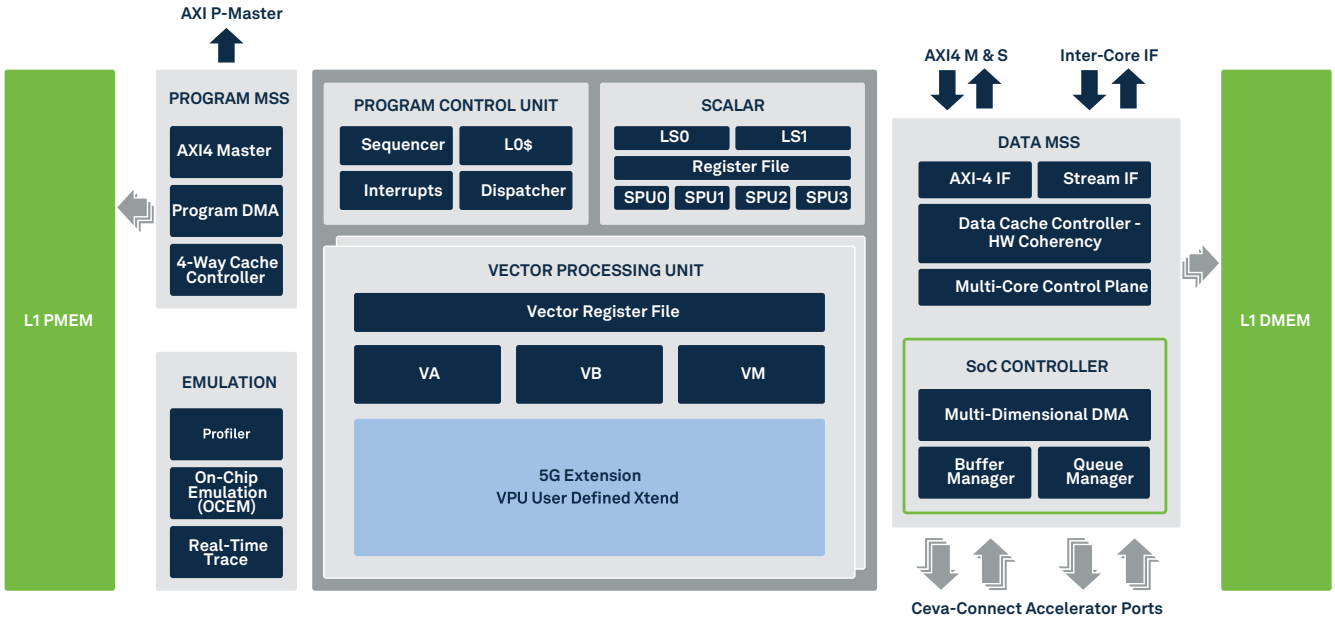
- **5G-NR & LTE-A Pro UE**
  - eMBB, URLLC
  - FWA (Fixed Wireless Access) CPE
  - C-V2X (Cellular V2X)
- **Wi-Fi 802.11ax/ac/ad Access Point**
- **V2X DSRC 802.11p**
- **Satellite modems**
- **Wireline G.Fast, G.hn. xDSL**

Cellular Modem HW accelerators available for Ceva-XC4500



Module	3G	LTE-A	LTE REL-12	3GPP-NR 5G
FFT /DFT		●	●	●
MLD MIMO Decoder		2x2, 4x4	2x2, 4x4	●
Vector Mac Unit			●	●
5G AI Processor				●
LLR Coprocessor		●	●	
Turbo-Decoder	●	●	●	
Viterbi Decoder	●	●	●	
5G LDPC Encoder/ Decoder				●
5G Polar Encoder/ Decoder				●
Fast Walsh –Hadamard Transform	●			
3G Despreader/ Descrambler	●			

Ceva-XC4500 5G architecture diagram



Architecture Highlights

- **Core features**
  - Runs at 1.2 GHz in 16nm.
  - Fully programmable DSP architecture incorporating unique mix of VLIW and SIMD vector capabilities
  - 13-stage pipeline enables very high speed for the most extreme use cases
  - 8-way VLIW provides optimal hardware utilization
  - Extremely powerful vector processor supports fixed- and floating-point operations with 64 MACs per cycle
  - Rich Instruction set supports multiple precision integer, pseudo FP and IEEE FP real and complex operations to offer the most appropriate precision vs performance tradeoff for specific algorithms
  - Dedicated instruction set (ISA) for 5G-NR eMBB UE and LTE-A Pro
- **System features**
  - AMBA 4 compliant matrix interconnect
  - Comprehensive multicore support with ACE-compliant cache coherency
  - Hardware/software partitioning delivers exceptional power efficiency while maintaining software flexibility with Queue and Buffer Managers and FIC interfaces
  - Rich set of optimized SW Libraries and HW Accelerators for 5G-NR, LTE-A Pro,3G, Wi-Fi 11ac/ax UE and AP

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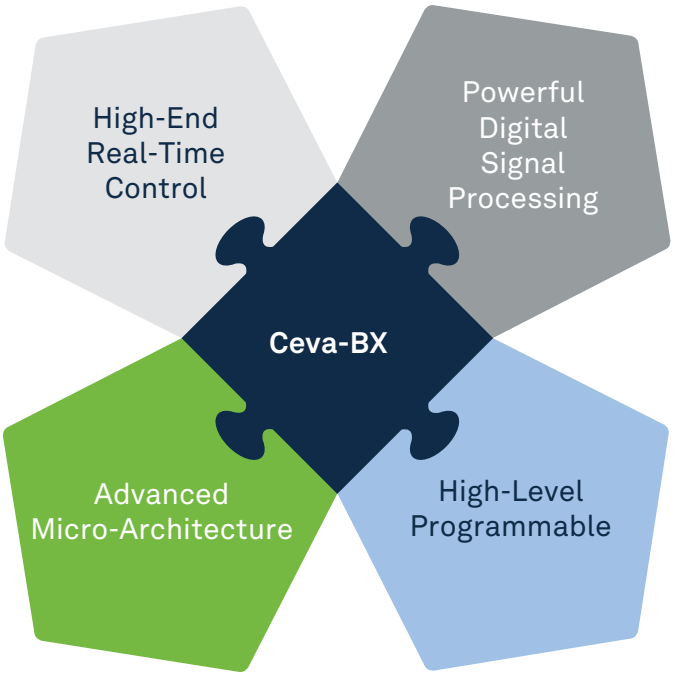
For more information:

High level programmable, modern processor architecture for a broad range of signal processing and control workloads

Ceva-BX2 is a multipurpose hybrid DSP and Controller designed for the inherent low power requirements of DSP kernels with high-level programming and compact code size requirements of a large control code base.



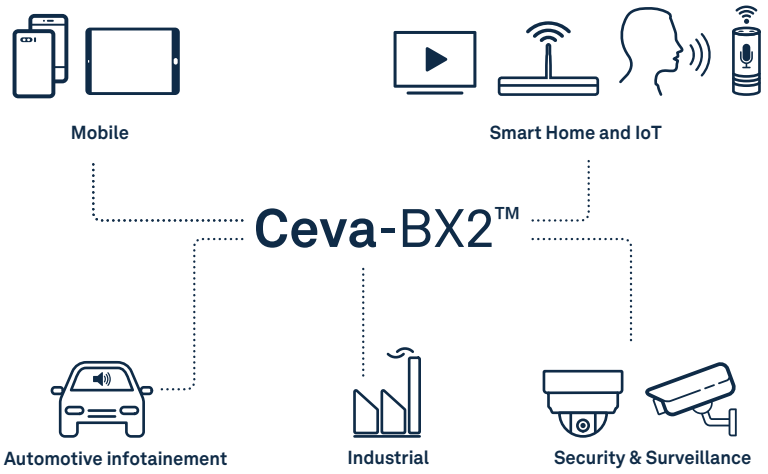
Key Benefits

- **Perfect alternative** for special purpose DSPs and MCUs with DSP coprocessors, allowing efficient handling of today's diverse algorithm needs
- **Fast software bring up** using a comprehensive tool chain and DSP libraries
- **Advanced Neural Network** support for deep learning at the edge
- **Compact code size** and **low power** using inbuilt mechanisms

Tools and Software Availability

- **Application specific ISA and software:**
  - ClearVox - multi-mic noise reduction
  - WhisPro - speech recognition
  - Cellular IoT and GNSS ISA
- **DSP and neural network compute libraries**
- **Common neural network frameworks support**
- **Advanced LLVM compiler**
- **Eclipse based debugger**
- **RTOS**

Target Markets



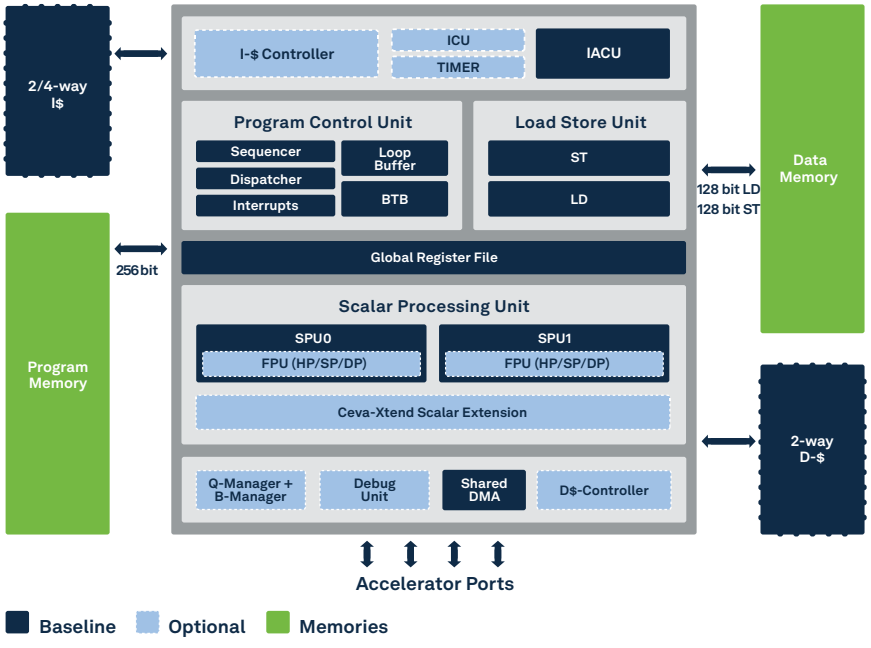
Multipurpose DSP/Controller

The Ceva-BX2 architecture delivers excellent all-round performance for a new generation of smart devices by offering a high performance hybrid architecture that is a single compute island for all DSP and control workloads.

Ceva-BX™2

Architecture Highlights

- **Powerful DSP performance**
  - 5-way VLIW
  - 8/16/32/64-bit data types
  - Quad 32x32 MACs
  - Octal 16x16 MACs
  - 16x8 and 8x8 Neural Network support
  - Half, single and double precision IEEE floating point units
- **High performance controller**
  - 4.5 CoreMark/MHz
  - Dynamic branch prediction
  - Full RTOS support
  - Secured execution modes
  - Compact code size
- **Advanced System Control**
  - Automatic buffer management
  - High QoS with queue managers
  - Dedicated HW accelerator ports
  - Advanced multi-way instruction and data cache subsystem



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