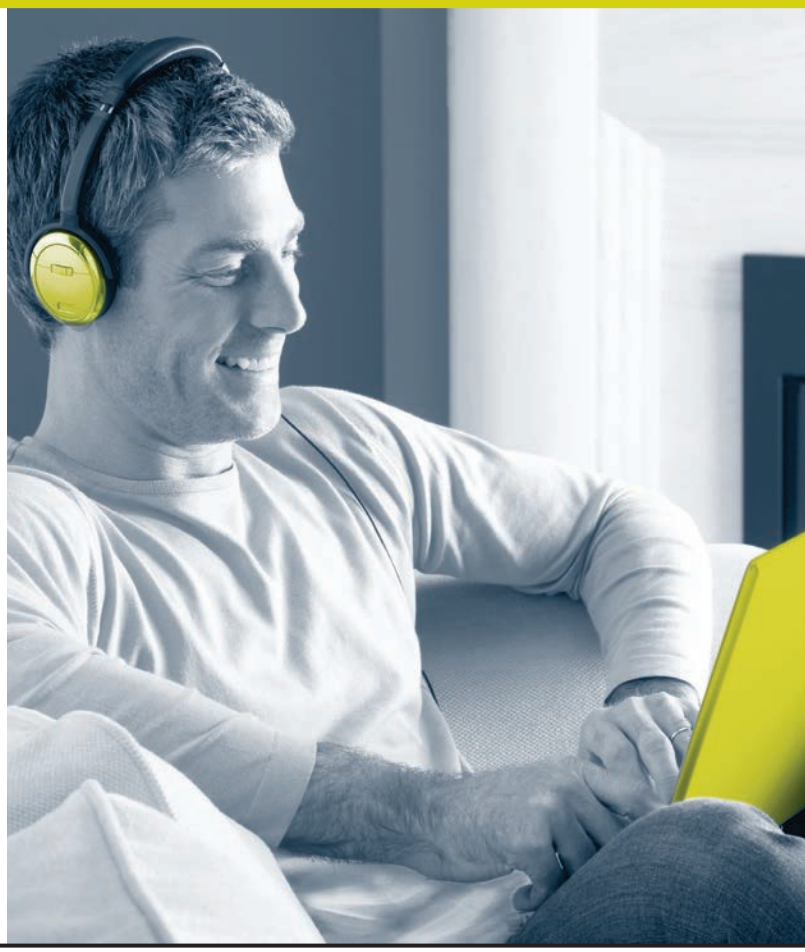
CEVA®
The DSP Powerhouse



CEVA-TEAKLITE-4

A MULTIFUNCTIONAL DSP ARCHITECTURE FOR HIGH-PERFORMANCE, LOW-POWER AUDIO/VOICE/SENSING AND WIRELESS COMMUNICATION APPLICATIONS

Features

- Small size and ultra-low-power
  - 90K gates area optimized
- Less than 20uW for always-on voice trigger @ 28nm
- High-performance
  - Up to 1.5 GHz @ 28nm HPM
- Full set of audio/voice/sensor-fusion software codecs and modules
- Native 32-bit, Harvard/SIMD architecture DSP with multiple options
  - Single/dual/quad 32x32-bit multipliers
  - Dual/quad 16x16-bit multipliers
  - 32-bit register file
  - 128-bit or 64-bit data memory bus width
  - Automatic 32-bit and 16-bit saturation
  - 64/72-bit support for wide dynamic range
  - Excellent controller capabilities
  - Optional user-defined instructions
  - Fully cached design and TCM support
- Easy software development
  - Optimizing C compiler
  - Cycle-accurate simulation and graphical profiling of the entire DSP sub-system
  - Macro assembler, linker, and GUI debugger
  - Tight MATLAB bi-directional connectivity

Benefits

- Scalable architecture frame work with four DSP cores for best match to various application needs
- CEVA-TeakLite-4 DSP cores can be used for applications that are highly sensitive to die-area and power consumption
- CEVA-TeakLite-4 DSP cores are ideal for multiple audio, voice, sensor-fusion and connectivity processing applications
- Fully integrated with CEVA-Bluetooth and CEVA-WiFi connectivity solutions
- Supported by a broad range of fully-certified HD-Audio and voice codecs
- CEVA-TeakLite-4 architecture is backed by an extensive SW and system partner network
- Smooth C-level software development and easy integration into target SoC reduces risk and time-to-market

CEVA'S TEAKLITE FAMILY IS THE WORLD'S MOST POPULAR DSP CORE AND HAS SHIPPED IN MORE THAN 3.5 BILLION DEVICES TO DATE!

The Always-on, Always-connected World

The market for high-performance, low-power, digital audio and voice processing applications is seeing tremendous changes. Mobile devices like smartphones and tablets are required to handle increasing audio and voice processing requirements such as super-wideband and full-band converged audio and voice use-cases, which are enabled by LTE and LTE-A cellular networks and services such as VoLTE. At the same time, users expect their devices to remain always-on, always-responsive, and constantly connected to their enterprise and personal digital cloud repositories. These accumulated requirements pose great challenges for SoC and device manufacturers.

Hands-free activation is becoming a 'must have' feature in a multitude of devices, primarily smartphones and wearables, and solutions have to operate efficiently and reliably to meet demanding consumer requirements. Be it voice control, gesture control or face unlock, a natural user interface (UI) is expected to be always-on in order to be totally hands-free and therefore it must be highly optimal and consume very little power. Even a relatively minor inefficiency could easily translate into a substantial power loss and significantly shorten battery life as a consequence.

Sensing is another key feature of smartphones, tablets, wearables and IoT devices. Combined processing of sensory data from disparate sources, also known as Sensor Fusion, has proven to provide valuable contextual awareness, motion-based gesture control and indoor navigation capabilities for a host of user applications. Multiple MEMS sensors such as 9-Axis motion sensors, barometers, thermometers and more call for a high-precision sensor fusion DSP to accurately deduct motion and environmental data, and eliminate false readings. Efficiency and power consumptions are of the essence as well, as sensor fusion is often an always-on type of task.

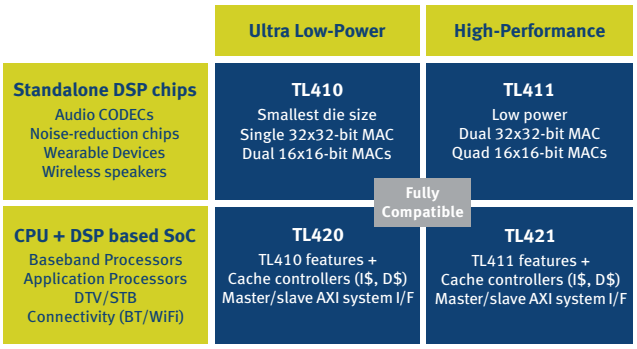
In the case of internet-enabled Smart TVs, STB devices, and a host of OTT streaming services, it is necessary to support an extremely wide range of audio codecs. In addition to mainstream codecs like MP3, AAC, WMA, Vorbis, coupled with advanced post-processing techniques, it is also necessary to support compute-intensive lossy and lossless HD Audio codecs, including the latest object-based audio processing standards, which enable exact rendering of complex 3D audio scenes, but at the expanse of greatly increased algorithmic complexity.

Wireless connectivity is related to all of the above markets and is constantly growing in coordination with market growth for mobile devices and their wireless peripherals. Propelled by their popularity in those devices, the dominating wireless standards, namely Bluetooth and WiFi, have also proliferated into adjacent markets such as wearable devices, smart home, smart cars etc. which are often collectively referred to as the Internet of Things (IoT). Since the introduction of Bluetooth Low-Energy (BLE) by the Bluetooth Special Interest Group (SIG) in V4.0, BLE can be found in numerous IoT products thanks to its superior power consumption comparing to other wireless standards. This further positions Bluetooth as the most common low-throughput standard while Wi-Fi remains the standard of choice when higher throughput is required. Additional wireless standards, such as Zigbee for example, offer slightly different mixes of range, throughput, area, power consumption and cost and can therefore coexist alongside Bluetooth and Wi-Fi or even displace them in some use cases.

The Solution is the CEVA-TeakLite-4

The CEVA-TeakLite Family of DSP cores is designed to address the needs of high volume, cost-sensitive markets. Founded on a classic direct memory access-based architecture, the CEVA-TeakLite family combines small die size, high code density, and high performance.

The fourth generation of the CEVA-TeakLite family, the CEVA-TeakLite-4 is a low-power, native 32-bit, variable 10-stage pipeline, fixed-point DSP architecture framework. The CEVA-TeakLite-4 is a fully synthesizable, process-independent design that allows the SoC designer to select the optimal implementation in terms of silicon area, power consumption, and operating frequency.



Target Applications

Thanks to its scalability, the CEVA-TeakLite-4 DSP family is efficiently handling most demanding audio, voice, sensing and wireless connectivity use-cases, whether targeting ultra-low-power always-on functions, advanced multi-microphone voice processing, or high-performance multichannel audio processing and post-processing. CEVA-TeakLite-4 cores are adopted by mobile, home, and automotive chip vendors, ranging from the smallest, lowest-power audio CODEC and voice activation chips, to Baseband, Application Processors and connectivity chips, to high-end audio such as wireless speakers, digital televisions (DTVs), set-top boxes (STBs), game consoles, and more.

Always-on User Interface (UI)

The CEVA-TeakLite-4 offers multi-functional DSP capabilities, making it ideal for implementing always-on solutions that often include intensive signal processing algorithms such as those used for voice recognition and face detection. Furthermore, latest generation power scaling technology of the CEVA-TeakLite-4 V2 enables it to run always-on UI with ultra-low power consumption by shutting down unneeded hardware on a cycle-by-cycle basis. Being CEVA's smallest DSP core, it also benefits from very low leakage power, which is especially important when implementing always-on functionality, such as that of a voice trigger chip for example.

Sensor-Fusion

The CEVA-TeakLite-4 boasts a highly optimized arithmetic ISA as well as a rich control ISA that are efficiently utilized by the compiler as it handles Sensor Fusion code, which often mixes arithmetics and control. Furthermore, with its power-optimized hand-crafted RTL and power scaling technology, the CEVA-TeakLite-4 consumes ultra-low power by design and is therefore fully geared for ultra-low power sensor fusion processing.

Audio and Voice

Audio/voice CODECS (ADC, DAC, D-Class amplifiers, noise reduction, audio hubs) are shifting from hardware-based digital filters/equalizers to using a programmable DSP. This is because programmable DSPs are better suited to handle the ever-changing demands for diverse, high-complexity, evolving algorithms used for tasks like multi-microphone beam-forming, noise reduction for voice communication and voice recognition support, and audio post-processing for speaker correction, virtual surround sound, and an overall improved audio experience.

Mobile application processors are required to handle ever-increasing audio and voice processing requirements, including multi-channel and object-based audio decode (music and gaming), voice pre-processing (e.g. noise reduction), audio post- processing (e.g. Dolby DS1), and wideband and super- wideband vocoders (e.g. VoLTE and EVS). In these cases, it is common practice today to offload the main CPU and implement the computationally-intensive audio and voice processing algorithms using a dedicated audio DSP. This dramatically reduces the power consumption of the system and frees up 100s of megahertz on the main CPU. In this case, chip vendors require a scalable DSP architecture (e.g. single/dual/quad 32-bit MACs) to address a wide range of applications, coupled with an open DSP architecture to facilitate customization and differentiation by their OEM customers.

In the case of automotive infotainment systems and home entertainment systems such as connected DTV, STB, and gaming devices, these systems must support multiple high-definition audio standards, advanced audio post-processing, and wide-band voice communication/UI. In recent years, the focus has moved away from simply providing multi-stream, multi-channel audio codecs to providing a wide variety of computationally intensive pre- and post-processing capabilities, such as audio post-processing (virtual surround sound, speaker correction), and complex living room and automotive voice processing (multi-microphone noise reduction, voice command, conferencing, etc.).

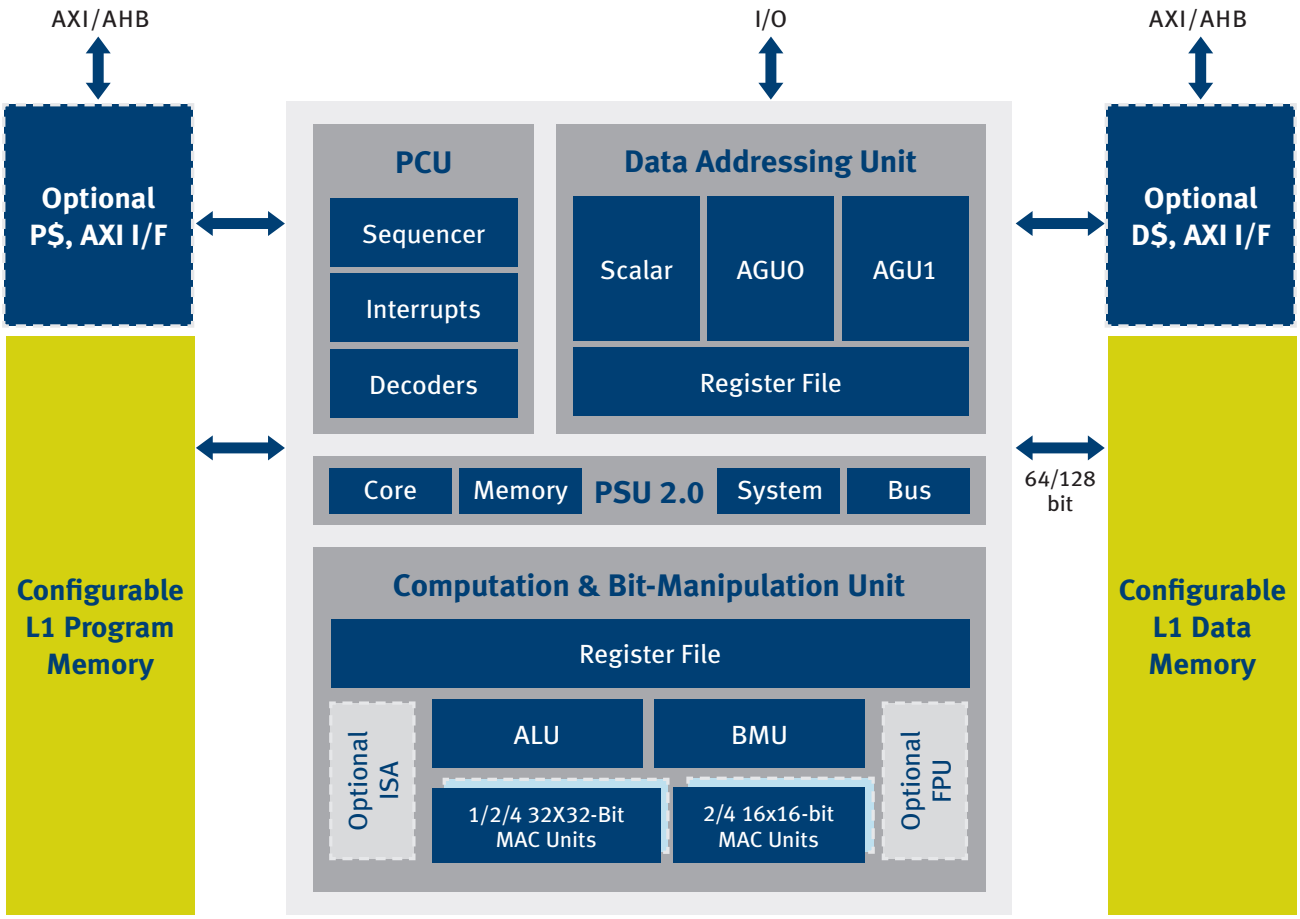
Wireless Connectivity

Combined with the CEVA-Bluetooth or CEVA-WiFi hardware and software solutions, the CEVA-TeakLite-4 enables a wide range of wireless applications without requiring an additional CPU. A smartwatch solution, for example, can use a single Bluetooth-enabled CEVA-TeakLite-4 to run always-on voice

activation and voice commands, sensor fusion functionality, audio/voice processing and dual mode Low Energy Bluetooth (also known as Bluetooth Smart Ready) capable of both BLE such as that of Bluetooth Smart, and wireless audio. Given the highly integrated nature of IoT solutions, such a capacity cannot be overestimated. On top of Bluetooth and WiFi, other popular standards such as Zigbee are also supported where every wireless standard can be used either as standalone or as a combo solution while coexisting with the other standards. For example, a wireless speaker solution combining both a WiFi speaker and a Bluetooth speaker can have both Bluetooth and WiFi audio using a single Bluetooth and WiFi enabled CEVA-TeakLite-4.

The CEVA-TeakLite-4 architecture addresses all of these applications and markets. With a primary target of standalone DSP chips used to implement audio CODECs, voice activation, sensor-hub and noise-reduction chips, the ultra-low-power CEVA-TL410 DSP core offers the smallest die size with its single 32x32-bit MAC, dual 16x16-bit MACs, and simple memory interface. If higher performance is required, the CEVA-TL411 core provides dual 32x32-bit MACs and quad 16x16-bit MACs.

Alternatively, for CPU + DSP-based SoCs, such as the application processors and main SoCs used in smartphones, digital televisions (DTVs), set-top boxes (STBs), and game consoles, the CEVA-TL420 augments the features of the



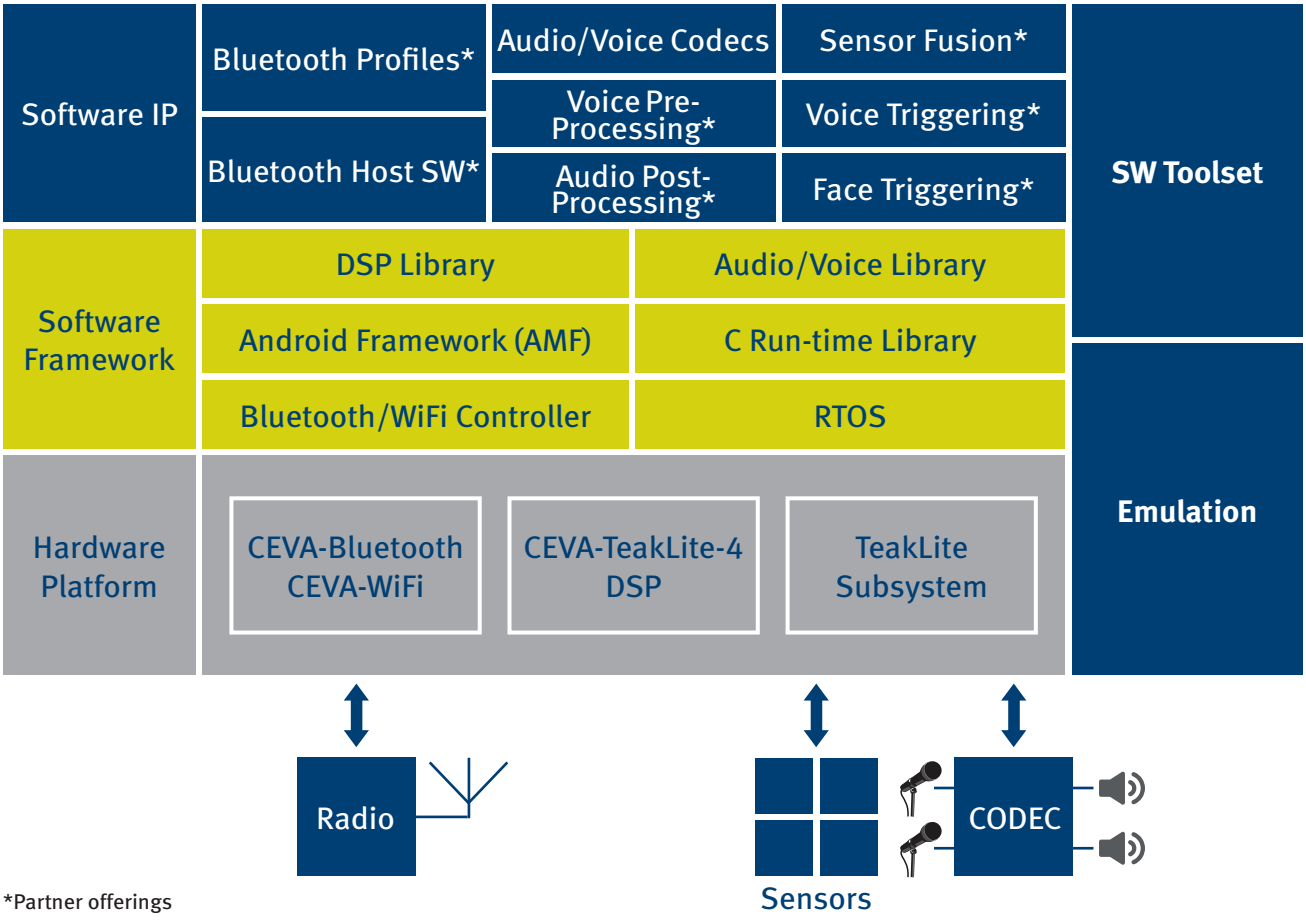
CEVA-TL410 with data and instruction cache controllers and a master/slave AXI system interface (the CEVA-TL421 augments the CEVA-TL411 with the same high-end capabilities). All CEVA-TeakLite-4 architecture-compliant cores are fully compatible with each other and with previous generation CEVA-TeakLite family cores.

Putting it all Together

In many of the markets mentioned above, such as mobile and wearable devices for example, there is a need for all or most of the above mentioned functions and in some use cases they should even run simultaneously. To this end, a single CEVA-TeakLite-4 can run all those functions concurrently using a task scheduler or an RTOS and still provide headroom for additional user software. For example, the CEVA-TeakLite-4 runs various always-on functions simultaneously in less than 150uW at a 28nm HPM process node: voice trigger, face trigger, sensor fusion and BLE. Running similar functions on the application processor would require at least two orders of magnitude more power, clearly surpassing the power consumption threshold required for a reasonable battery life.

High-Performance, Energy-Efficient, Scalable Architecture

The CEVA-TeakLite-4 architecture is optimized for standalone



*Partner offerings

audio chips running filters, sensor-fusion, voice pre-processing, audio post- processing, and noise reduction; also for mobile applications such as off-loading the main CPU by performing multi-channel audio decode, transcoding, voice pre-processing, and audio post-processing under the Android or Windows Phone operating systems. The CEVA-TeakLite-4 architecture framework is scalable and supports user differentiation to allow expansion for handling proprietary algorithm acceleration and future use-cases.

An audio ISA (instruction set architecture) providing dedicated audio instructions is present in all CEVA-TeakLite-4-based cores. Also, all members of the family include an integrated Power Scaling Unit (PSU 2.0) for smart power management.

CEVA-TeakLite-4 DSP cores support multiple voltage domains associated with the main functional units, such as the DSP logic, the program and data caches, and so forth. The core also supports multiple operational modes ranging from full operation, to debug bypass, to memory retention, to complete power shut-off. Furthermore, the AXI full duplex buses also offer low-power features, such as ability to shut down when no data traffic is present.

Effortless Software Development

The ability to program in C is essential for reducing development time and ensuring easy portability to future platforms. The CEVA-TeakLite-4 architecture is compiler-

Voice	Audio	HD-Audio
G.723	MP3	Dolby TrueHD
G.729	MP3Pro	Dolby Digital Plus
G.728	Ogg Vorbiss	Dolby Digital decoder (AC3)
G.729.1	MPEG4 AAC LC	Dolby Digital encoder (DDCE)
G.722	HE AAC V1	Dolby ProLogic IIx
G.726	HE AAC V2	Dolby MS10/MS11
G.727	HE-AAC V2 5.1 Ch	Dolby Volume
G.168	MPEG4 AAC BSAC	Dolby DS1
G.161	WMA8	
iLBC	WMA9	DTS HD-Audio
AMR-NB	WMA10	DTS Master Audio
HR	WMA10Pro	DTS High Resolution
FR	RealAudio8	DTS Low Bit Rate
AMR-WB	RealAudio9	DTS Extended Surround
EVRC	RealAudio10	DTS 96/24
EVRC-B	SBC	DTS Digital Surround
EVRC-C	FLAC	DTS Transcoder
QCELP	CELT	DTS Neo:6
SMV	DRA	DTS M6
SILK (32-bit)		DTS M8
EVS		

aware, implementing an orthogonal instruction set and operands so as to ensure optimal utilization of the processor capabilities from the C level. CEVA-TeakLite-4 processors are supported by a complete software development, debug, and optimization environment in the form of the CEVA-Toolbox™. CEVA-Toolbox is an advanced Integrated Development Environment (IDE), which includes a powerful compiler that facilitates software development without the need for users to master architecture-specific details. An integrated simulator provides accurate and efficient verification of the entire system including the memory sub-systems. In addition, CEVA-Toolbox includes libraries, a graphical debugger, and a complete optimization tool chain named CEVA Application Optimizer. The Application Optimizer enables automatic optimizations applied in the C source code.

The CEVA-TL410, CEVA-TL411, CEVA-TL420, and CEVA-TL421 DSP cores are supported by a wide range of deliverables, which significantly reduces risk and time-to-market. These deliverables include a complete implementation along with associated hardware and software development tools and verification and simulation environments. CEVA-TeakLite-4-based designs can also be implemented in an FPGA for prototyping and system integration.

The CEVA-TeakLite-4 is also backed up by a wealth of software and algorithms. For example, CEVA offers more than 100 audio and voice codecs for the TeakLite family DSP cores.

All of these codecs are fully developed and supported by CEVA. To further reduce the cost, complexity, and risk in bringing products to market, CEVA has established an ecosystem of partners who provide application software, RTOS modules, reference designs, complementary IP, design services, and complete solutions based on CEVA's DSP cores and Platforms and Solutions. Some example partner technologies are as follows:

Audio post-processing technologies

- Dirac – Dirac HD Sound
- KORG – 3D positional audio (gaming)
- Waves – MaxxAudio
- Qsound – Qsurround
- DTS – TruSurroundHD
- Dolby – DS1
- Arkamys – ImmerseU (portable), Sound Staging (automotive)

Voice pre-processing technologies

- Alango – Voice Communication Package
- NXP Software – LifeVibes VoiceExperience
- Asahi Kasei – voice pre-processing (noise reduction)
- DiMagic – noise/echo cancellation
- Waves – MaxxVoice
- Acoustic Technologies – SoundClear

Always-on technologies

- Sensory – voice activation
- Cywee Motion – sensor fusion
- Rubidium – voice activation
- Visidon – face detection

Android Multimedia Framework

The CEVA Android Multimedia Framework (AMF) is designed for Android system integrators, addressing the growing need for higher multimedia performance, longer battery life and quick time-to-market of multi-processor systems implementing the Android OS. Android system designers can easily harness the AMF, which is provided as a full reference design, to seamlessly offload audio, voice and speech from the CPU to the CEVA-TeakLite-4 DSP and improve power consumption in an order of magnitude as a result. It also enables Android programmers, even ones without DSP expertise, to use high-level languages to program the DSP, which is often out of reach without such a framework

State-of-the-Art Prototyping Platform

Today's increasingly complex SoC designs require development teams to have the ability to verify the design before taping out the actual silicon. CEVA offers a complete hardware-based development platform including development boards that assist system and software designers in validating their SoC application designs.

CEVA provides a dedicated ASIC to FPGA design flow and development boards that allows users to take "black box" instantiations of CEVA DSP cores and use them in FPGA- based prototyping systems. Additionally, the CEVA-TeakLite- III full-speed silicon, which is CEVA-TeakLite-4 compatible, provides a means for real-time algorithm development. The hardware platforms interface to a host PC via a JBox JTAG interface, thereby providing full application control including all required functionalities, such as breakpoints, real-time tracing, profiling, etc.

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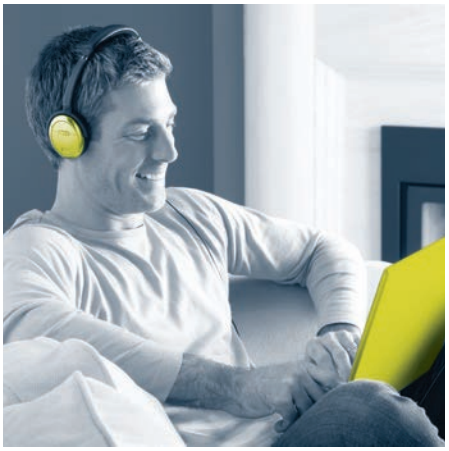

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