Enabling Deep Learning and Artificial Intelligence in Low-Power Embedded Devices

CEVA-XM6 is the 5th generation imaging and computer vision processor IP from CEVA, designed to bring deep learning and artificial intelligence capabilities to low-power embedded systems.
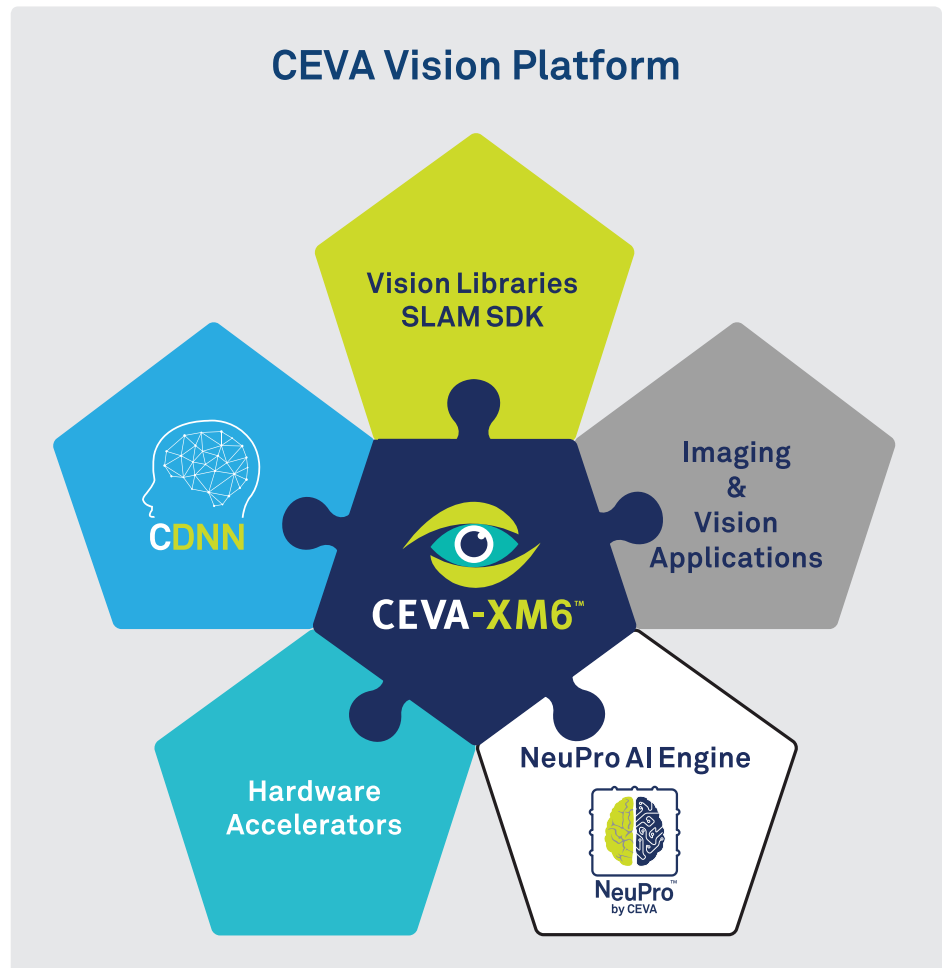
Key Benefits

> **Breakthrough performance** for cutting-edge imaging and vision algorithms
> **Low power consumption** for portable, battery-powered devices, including use cases with multiple vision engines
> **Flexible and scalable** to efficiently address the constantly evolving domain of intelligent vision
> **Small die size** for cost-effective mass market applications
> **Augmented by a comprehensive solution** to ease development cycle, accelerate time-to-market and enable product differentiation
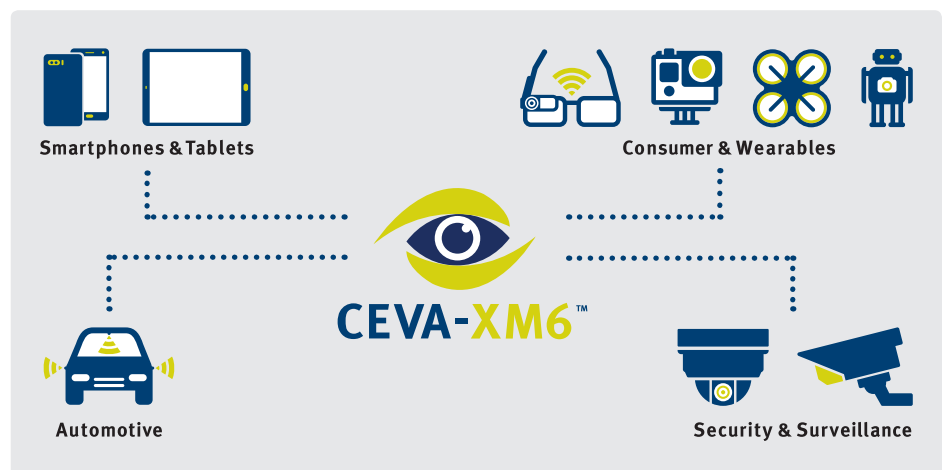
Key Metrics

> 1.5 GHz max frequency @28nm
> 8-way VLIW
> 128 (16x16-bit) MACs per cycle
> 4096-bit processing per cycle, utilizing only 512-bit memory bandwidth to save on power consumption
> Complemented by NeuPro engine provides compressive solution for CV and AI in a single platform

Integrated vision platform powered by CEVA-XM6 vision DSP:

CEVA Vision Platform

- Vision Libraries SLAM SDK
- CDNN
- Imaging & Vision Applications
- CEVA-XM6™
- Hardware Accelerators
- NeuPro AI Engine — NeuPro™ by CEVA

Target Markets

- Smartphones & Tablets
- Consumer & Wearables
- CEVA-XM6™
- Automotive
- Security & Surveillance

CEVA Vision Platform

Designing an intelligent embedded vision application has never been faster, easier or lower-risk, thanks to the comprehensive vision platform built around the CEVA-XM6 DSP. The platform includes the CEVA Deep Neural Network (CDNN) compiler graph, computer vision software libraries, and broad set of algorithms.

Automotive-ready

The CEVA-XM6 DSP is ISO 26262 active safety compliant and safety package deliverables. It supports the needs of next generation ADAS and automated driving solutions for automotive use cases.
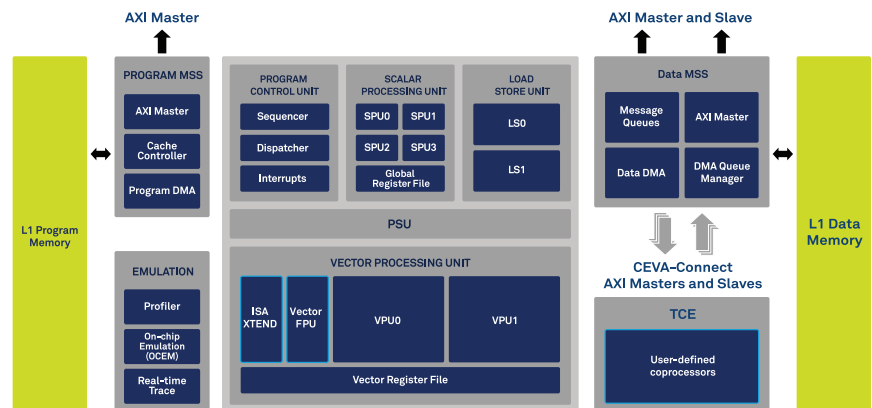
Architectural Highlights

> Innovative vector processor unit (VPU) architecture – ensuring above 95% MAC utilization

> Enhanced Parallel Scatter-Gather Memory Load Mechanism – further improving the performance of vision algorithms, including SLAM and depth mapping

> Sliding Window 2.0™ patented mechanism to cope with wider variety and increasing complexity of neural networks

> Optional 32-way SIMD vector floating-point unit including IEEE half precision standard and major non-linear operations enhancements

> Enhanced 3D data processing scheme for accelerated CNN performance

> Improved control code performance by 50%

> A new scalar unit which further reduces code size

> Multi-core and system integration support

Target Applications

CEVA-XM6 block diagram