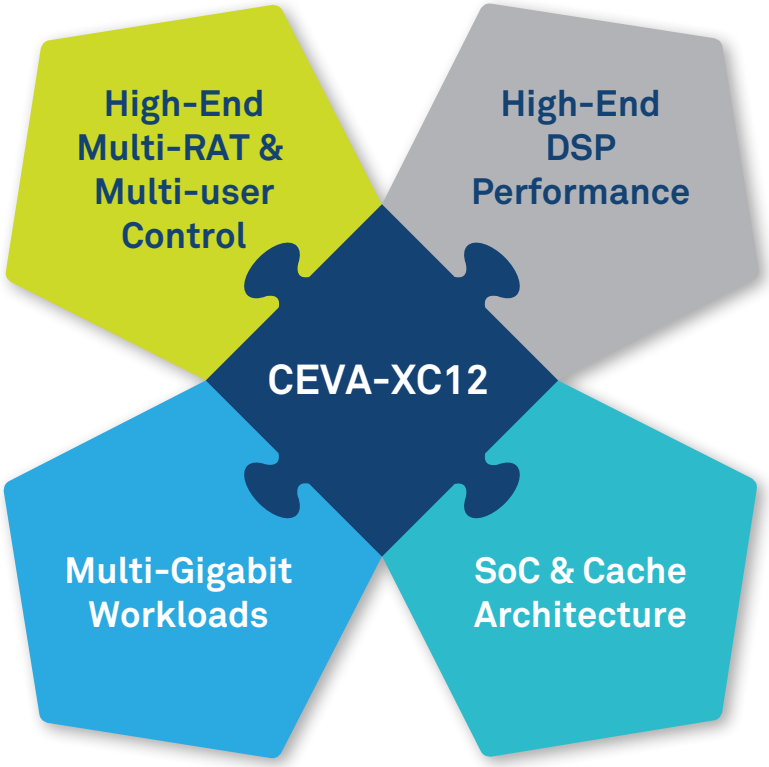
Enabling SDR based, multi-gigabit modems for 5G, LTE and Wi-Fi infrastructure

CEVA-XC12™ is fifth generation vector processor IP from CEVA, designed to bring multi-gigabit high-end communication and cellular capabilities to base-stations, gateways, access points and CPE.



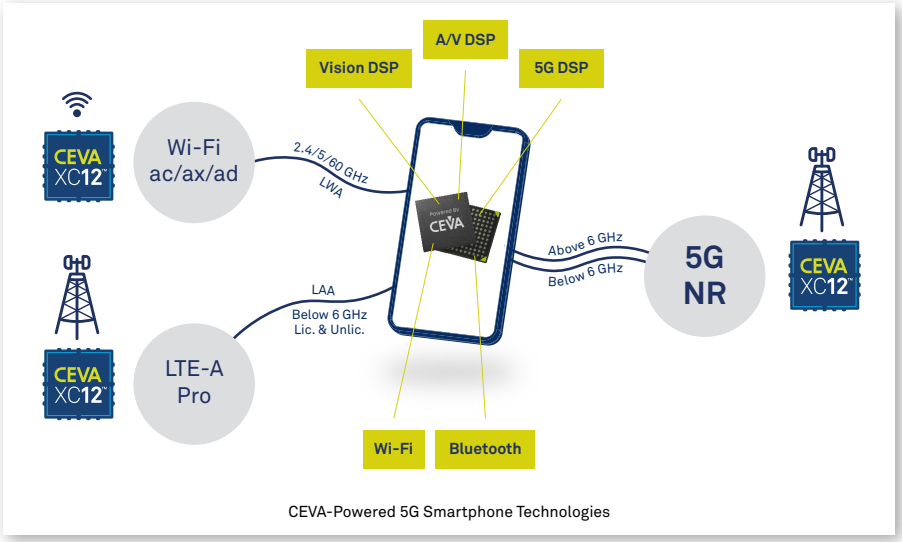
Key Benefits

- **Meets the demanding requirements** of extreme multi-gigabit communications use cases
- **Scalable architecture** addresses the full range of eNodeB and gNB from femtocell, small cell, macrocell, BBU & RRH to Cloud-RAN
- **Delivers up to 8x** more performance and consumes 50% less power than its CEVA-XC4500 predecessor
- **Quad-vector processor** addresses the needs of next-generation wireless applications such as 5G-NR, FWA, C-V2X, Wi-Fi 6 (802.11ax)

Applications and use-cases

- **5G-NR & LTE-A Pro infrastructure**
  - Cloud-RAN, BBU, RRH, Macrocell, Small Cell and Femtocell
  - FWA (Fixed Wireless Access) Small Cell and CPE
  - C-V2X (Cellular V2X)
- Wi-Fi 802.11ax/ac/ad Access Point
- Licensed Assisted Access (LAA)
- MulteFire carrier aggregation
- LTE/Wi-Fi Aggregation (LWA)

Target Markets

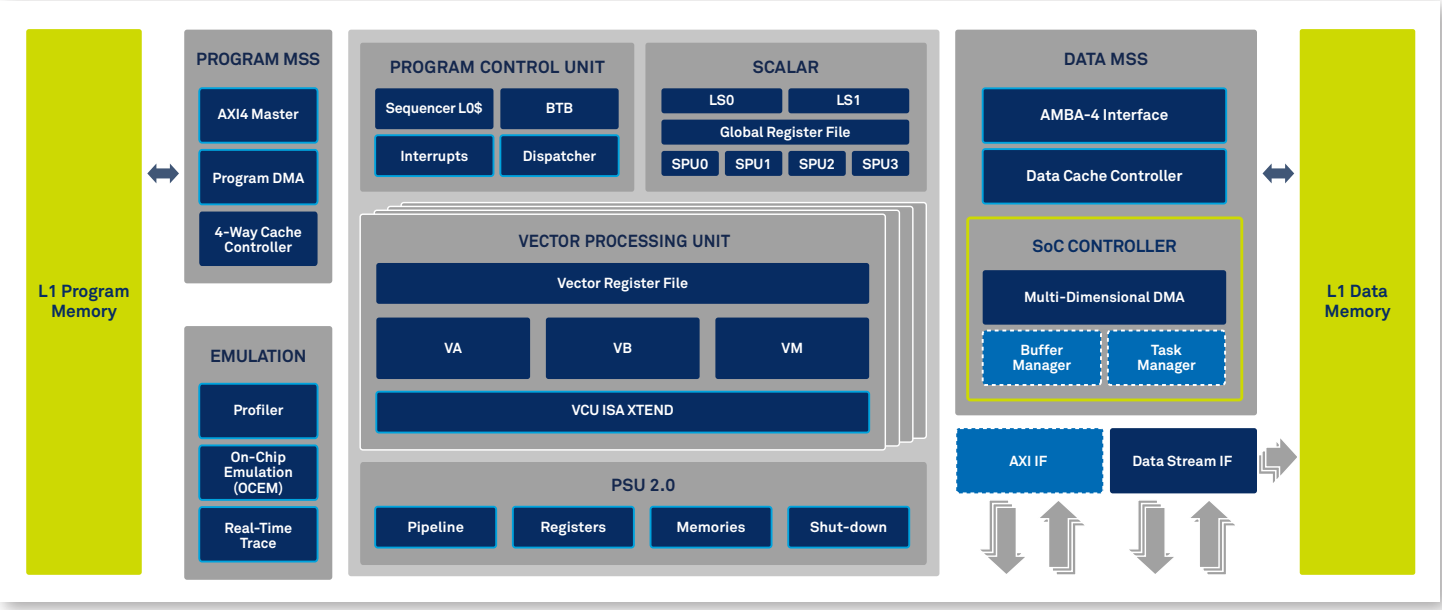


CEVA-Powered 5G Smartphone Technologies

Vector DSP

Massive MIMO processing with up to 256x256 matrix processing operators

CEVA-XC12 architecture diagram



Architecture Highlights

Core features

- Fully programmable DSP architecture incorporating unique mix of VLIW and SIMD vector capabilities
- 14-stage pipeline enables very high speed for the most extreme use cases
- 8-way VLIW provides optimal hardware utilization
- Extremely powerful vector processor supports fixed- and floating-point operations with 128 MACs per cycle
- Unique high-precision arithmetic optimized for matrix processing up to 256x256 and for non-linear operators
- Fully redesigned CPU/DSP SPU (Scalar Processing Unit) with optimizing C compiler for protocol, control, and DSP native C code
- SPU supports very low overhead RTOS multi-tasking with dynamic branch prediction
- Massive number of IoT/MTC users served by control plane

System features

- Core streaming interfaces support ultra-low latency
- AMBA 4 compliant matrix interconnect
- Comprehensive multicore support with ACE-compliant cache coherency
- Hardware/software partitioning delivers exceptional power efficiency while maintaining software flexibility with Queue and Buffer Managers and AXI interfaces

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