CEVA-XC5 / CEVA-XC323

Enabling Low Power Communications in Machine to Machine multi-mode endpoints

www.ceva-dsp.com

Introducing CEVA-XC5 / CEVA-XC323

- Low power communication DSPs designed to address the multi-mode connectivity requirements of M2M
  - Latest generation of highly popular CEVA-XC vector processor family, with already more than 30 licensees and tens of millions of devices shipped
- Target applications include wearalone wearables, smart grid, surveillance systems, asset tracking, remote monitoring systems, connected cars and smart utilities
- Supports every M2M standard including, LTE MTC Cat-1, Cat-0 and Cat-M standards, Wi-Fi 802.11n, PLC, 802.15.4g, ZigBee/Thread, GNSS, NB-IoT, LoRa, SIGFOX, Wi-Fi 802.11ah

Already in design for low power wireless M2M SoCs

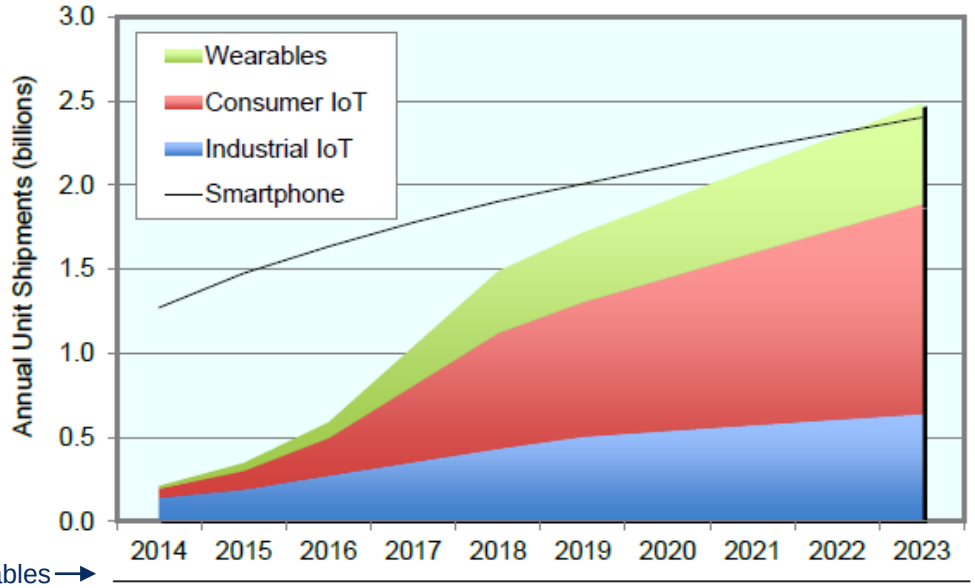
70%
Lower dynamic power consumption*

40%
Smaller*

20%
Reduction in memory size*

M2M Market Trends

- Today industrial smart meters dominate the M2M market
- By 2018, the consumer market will surpass industrial
  - Includes connected cars and appliances
- By 2020, 20% of M2M devices will use cellular technology in multiple segments
  - Connected cars emergency
  - Wearalone smartwatches
  - Smart meters
  - White appliances
  - Smart city security
  - Environmental sensors
  - Asset tracking



Source: The Linley Group: A Guide to Processors for IoT and Wearables

M2M/IoT Communications Challenges

Key Challenges

Flexibility
Many standards, some still under development
Specifications are not finalized and will require updates and remote upgrades in the field

Multi-mode
Most use-cases require multiple functions to run concurrently

PHY & Protocol require a high performance processor with true RTOS to minimize latencies

Extreme low power: 10 years on 2 AA batt

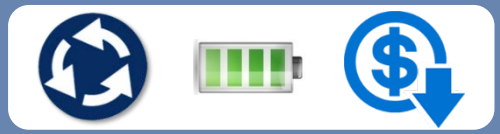
Very low cost: < $5 / module

Existing Solutions

HW centric modems
Can't be upgraded to track standards evolution and country variants ✗
Can't perform field updates ✗

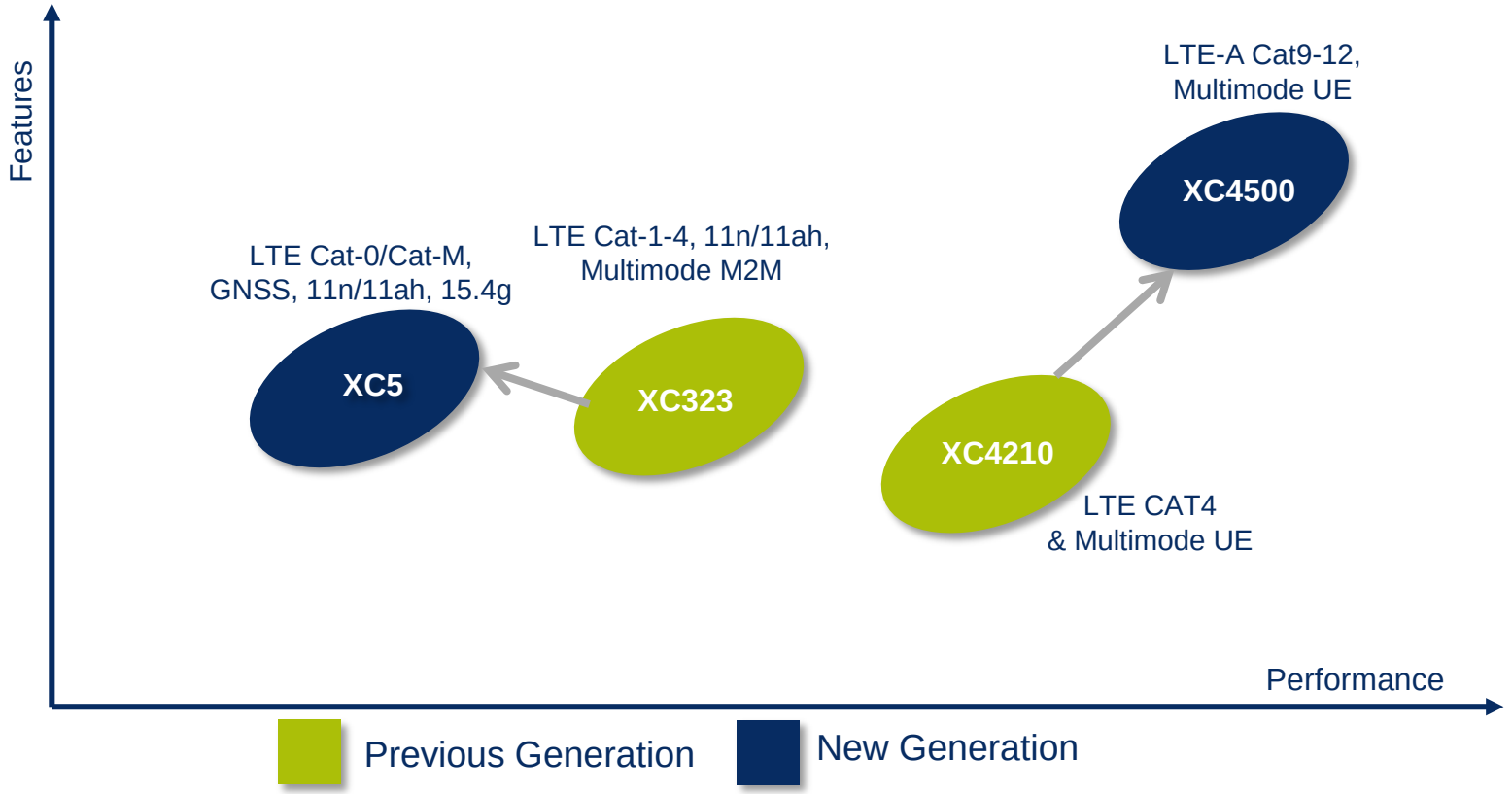
Multimode systems are heterogeneous
Piecewise collection of independent modems ✗
Sub-optimal area and cost ✗
Longer Time to Market ✗

Software Defined Modems (SDM) are required to address these challenges with low cost and low power solutions



CEVA-XC DSP Roadmap

Vector DSP for M2M and Cellular UE



CEVA-XC5/XC323 Architecture Highlights

DSP Core Features

- 8-way unrestricted VLIW
- Vector units with 16/32 MACs per cycle
- Dedicated communication ISA
- Flexible operation types on vector
  - 8/16/32-bit native data types
  - 64/32/16 operations per cycle accordingly
  - Inter-vector & intra-vector operations

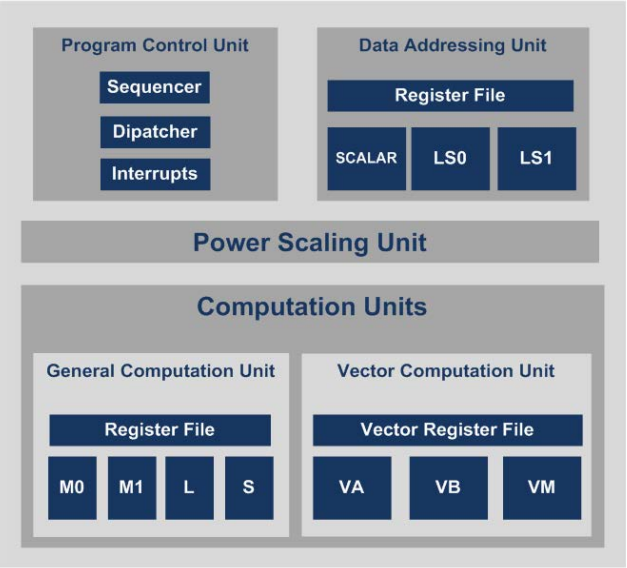
Memory and Subsystem Features

- 4-way set associative non-blocking program cache
- Powerful DMAs for instruction and data multi-core and system support
- PSU 2.0 - latest generation power scaling technology
  - Allows to further reduce power during LTE Cat-0/M long DRX and Power Saving Mode (PSM)

Highly efficient communication processor (perf/mm^2, perf/mW)
Based on silicon proven CEVA-XC323 DSP

CEVA-XC5/XC323 Core Highlights

- Highly powerful communication processor
  - Incorporates typical DSP capabilities with advanced vector processing units
    - CEVA-XC5 performs 16 MAC per cycle
    - CEVA-XC323 performs 32 MAC per cycle
  - 8-way unrestricted VLIW
    - Up to three vector units
    - Up to four general units
    - Dual load support
  - Powerful SIMD Vector Computation Unit



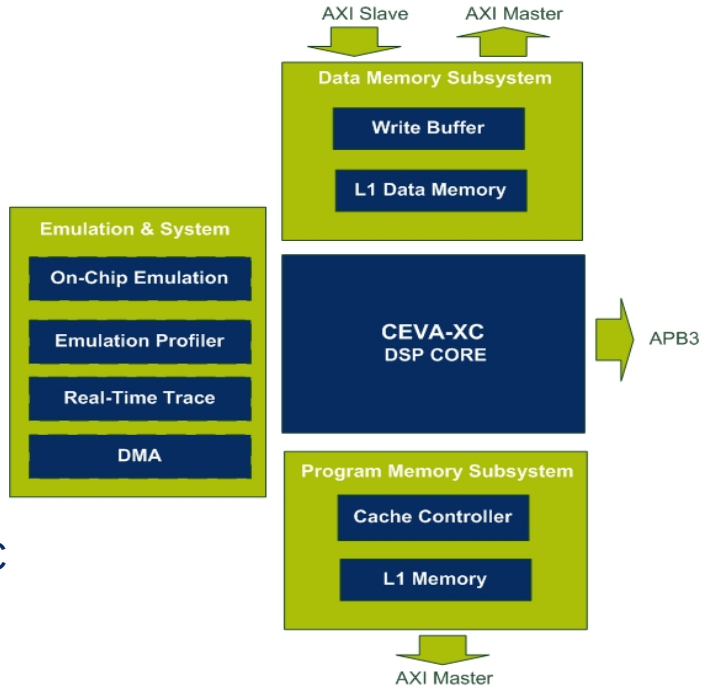
High ILP through a combination of SIMD and VLIW

Complete Memory Subsystem

CEVA-XC5/XC323 Memory Subsystem

Smooth Integration into Target SoCs

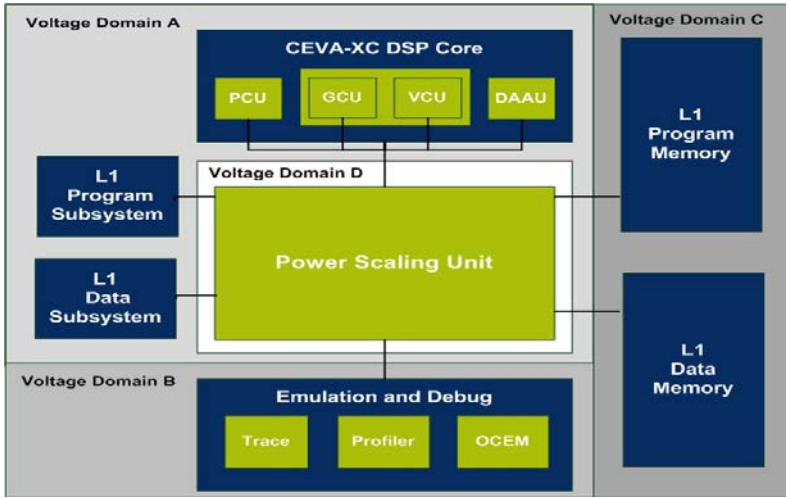
- AXI master and slave system buses
  - Supports Low Power Interface protocol
  - APB3 interface for slow devices
- Program cache
  - Reduces internal program memory size
- DMA controller
  - Background data transfers, de-interleaving
- Full Debug support
  - On Chip Emulation Module – debug connectivity to host PC
  - Real Time Trace – full debug of the application flow in RT
  - HW Profiler– helps pinpointing application bottlenecks



The MSS ensures optimal performance in real systems

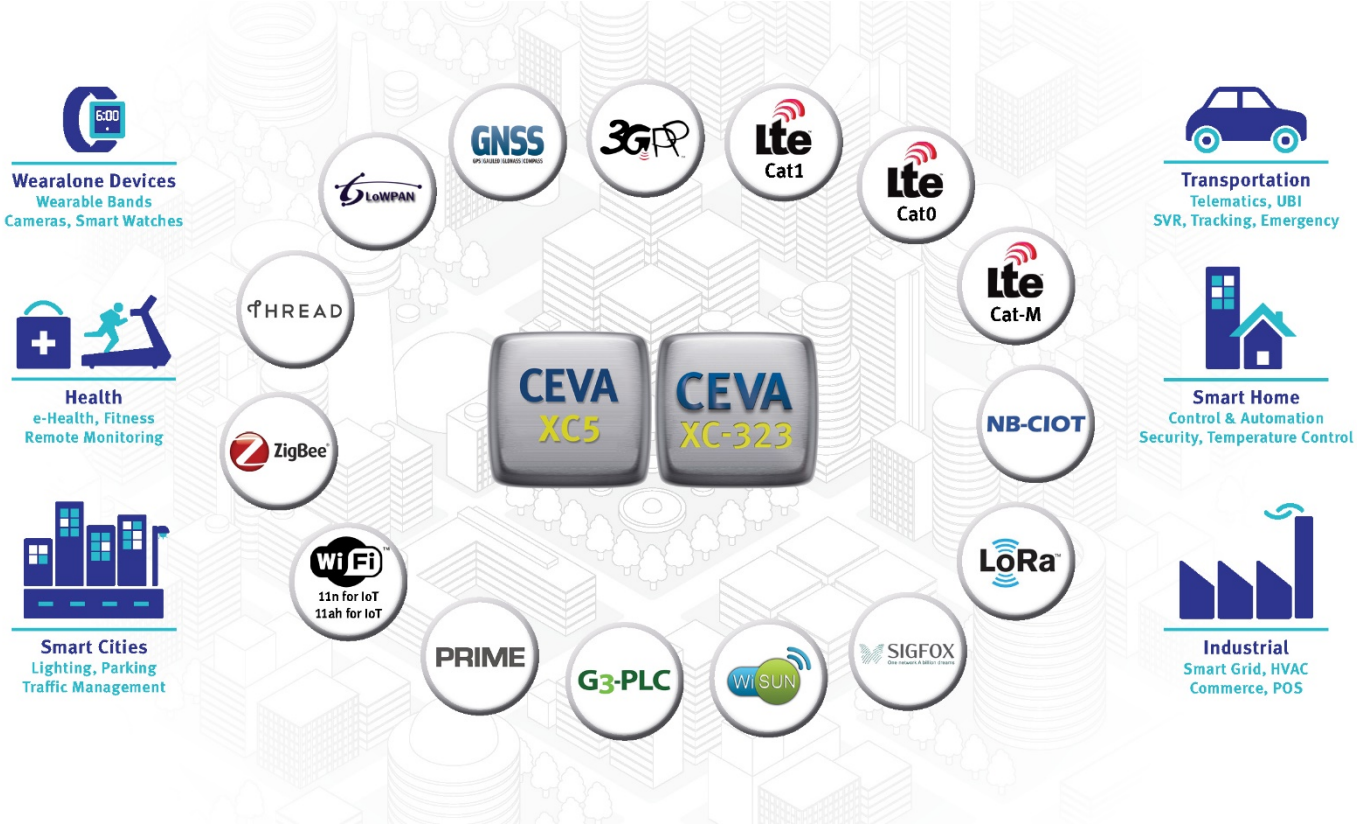
CEVA-XC5/XC323 Power Scaling Unit

- PSU supports multiple clock sources:
  - DSP Core
    - Internal power unit manages the clock automatically
    - High-level of granularity allows clocks shut-down for each block
  - Memory subsystem
  - Data and Program L1 Memories
  - Emulation & Debug modules
- PSU supports multiple voltage domains:
  - DSP Core and Memory subsystem
  - Data and Program L1 Memories
    - Enables data retention when the core is powered off
  - Emulation & Debug modules
    - Cutting voltage supply to OCEM, RTT & Profiler results in significant reduction in leakage power



PSU in both
CEVA-XC5 & CEVA-XC323

CEVA-XC5/XC323
Addressing Global M2M/IoT Connectivity



Thank You

For more information, visit www.ceva-dsp.com/M2M